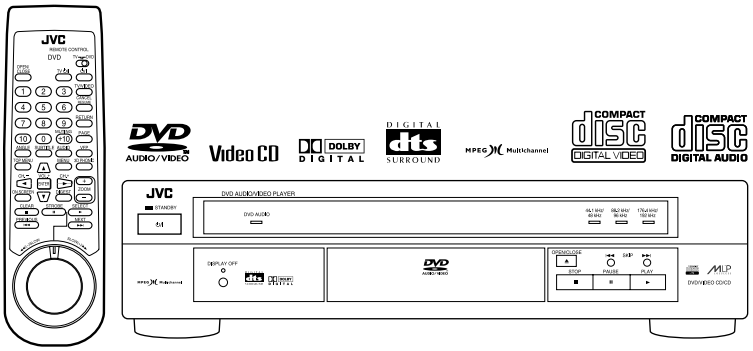
JVC

SERVICE MANUAL

DVD AUDIO/VIDEO PLAYER

XV-D721BK
XV-D723GD



Area Suffix	
XV-D721BK	
J	U.S.A
C	Canada
EG	Germany
ES	Spain
EN	Northern Europe
EE	Russian Federation
1U	US Minitary

Area Suffix	
XV-D723GD	
A	Australia
J	U.S.A
EG	Germany
ES	Singapore
EN	Northern Europe
UF	China
4U	Brazil,Mexico,Peru

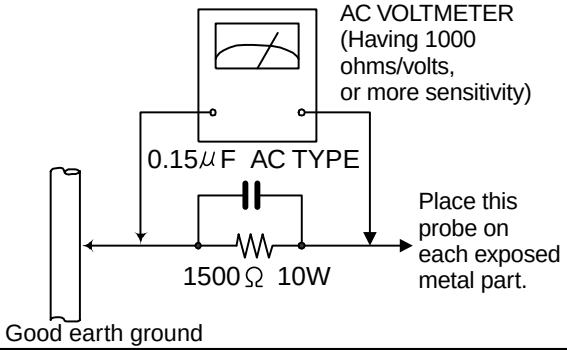
Contents

This service manual is printed on 100% recycled paper.

No.A0002
Nov. 2000

Safety Precautions

1. This design of this product contains special hardware and many circuits and components specially for safety purposes. For continued protection, no changes should be made to the original design unless authorized in writing by the manufacturer. Replacement parts must be identical to those used in the original circuits. Services should be performed by qualified personnel only.
2. Alterations of the design or circuitry of the product should not be made. Any design alterations of the product should not be made. Any design alterations or additions will void the manufacturer`s warranty and will further relieve the manufacture of responsibility for personal injury or property damage resulting therefrom.
3. Many electrical and mechanical parts in the products have special safety-related characteristics. These characteristics are often not evident from visual inspection nor can the protection afforded by them necessarily be obtained by using replacement components rated for higher voltage, wattage, etc. Replacement parts which have these special safety characteristics are identified in the Parts List of Service Manual. Electrical components having such features are identified by shading on the schematics and by (⚠) on the Parts List in the Service Manual. The use of a substitute replacement which does not have the same safety characteristics as the recommended replacement parts shown in the Parts List of Service Manual may create shock, fire, or other hazards.
4. The leads in the products are routed and dressed with ties, clamps, tubings, barriers and the like to be separated from live parts, high temperature parts, moving parts and/or sharp edges for the prevention of electric shock and fire hazard. When service is required, the original lead routing and dress should be observed, and it should be confirmed that they have been returned to normal, after re-assembling.
5. Leakage currnet check (Electrical shock hazard testing)
   After re-assembling the product, always perform an isolation check on the exposed metal parts of the product (antenna terminals, knobs, metal cabinet, screw heads, headphone jack, control shafts, etc.) to be sure the product is safe to operate without danger of electrical shock.
   Do not use a line isolation transformer during this check.
   - Plug the AC line cord directly into the AC outlet. Using a "Leakage Current Tester", measure the leakage current from each exposed metal parts of the cabinet , particularly any exposed metal part having a return path to the chassis, to a known good earth ground. Any leakage current must not exceed 0.5mA AC (r.m.s.)
   - Alternate check method
     Plug the AC line cord directly into the AC outlet. Use an AC voltmeter having, 1,000 ohms per volt or more sensitivity in the following manner. Connect a 1,500Ω 10W resistor paralleled by a 0.15μF AC-type capacitor between an exposed metal part and a known good earth ground.
     Measure the AC voltage across the resistor with the AC voltmeter.
     Move the resistor connection to eachexposed metal part, particularly any exposed metal part having a return path to the chassis, and meausre the AC voltage across the resistor. Now, reverse the plug in the AC outlet and repeat each measurement. voltage measured Any must not exceed 0.75 V AC (r.m.s.). This corresponds to 0.5 mA AC (r.m.s.).



Warning

1. This equipment has been designed and manufactured to meet international safety standards.
2. It is the legal responsibility of the repairer to ensure that these safety standards are maintained.
3. Repairs must be made in accordance with the relevant safety standards.
4. It is essential that safety critical components are replaced by approved parts.
5. If mains voltage selector is provided, check setting for local voltage.

⚠ ***CAUTION*** **Burrs formed during molding may be left over on some parts of the chassis. Therefore, pay attention to such burrs in the case of preforming repair of this system.**

Preventing static electricity

Electrostatic discharge (ESD), which occurs when static electricity stored in the body, fabric, etc. is discharged, can destroy the laser diode in the traverse unit (optical pickup). Take care to prevent this when performing repairs.

1.1. Grounding to prevent damage by static electricity

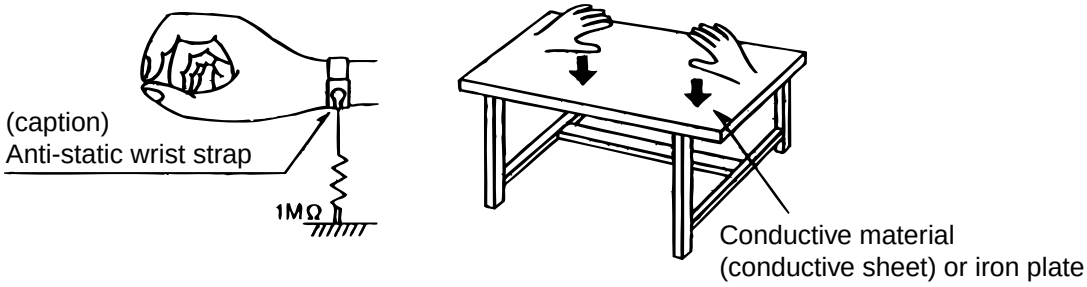
Static electricity in the work area can destroy the optical pickup (laser diode) in devices such as DVD players. Be careful to use proper grounding in the area where repairs are being performed.

1.1.1. Ground the workbench

1. Ground the workbench by laying conductive material (such as a conductive sheet) or an iron plate over it before placing the traverse unit (optical pickup) on it.

1.1.2. Ground yourself

1. Use an anti-static wrist strap to release any static electricity built up in your body.



1.1.3. Handling the optical pickup

1. In order to maintain quality during transport and before installation, both sides of the laser diode on the replacement optical pickup are shorted. After replacement, return the shorted parts to their original condition. (Refer to the text.)

2. Do not use a tester to check the condition of the laser diode in the optical pickup. The tester's internal power source can easily destroy the laser diode.

1.2. Handling the traverse unit (optical pickup)

1. Do not subject the traverse unit (optical pickup) to strong shocks, as it is a sensitive, complex unit.

2. Cut off the shorted part of the flexible cable using nippers, etc. after replacing the optical pickup. For specific details, refer to the replacement procedure in the text. Remove the anti-static pin when replacing the traverse unit. Be careful not to take too long a time when attaching it to the connector.

3. Handle the flexible cable carefully as it may break when subjected to strong force.

4. It is not possible to adjust the semi-fixed resistor that adjusts the laser power. Do not turn it

Important for Laser Products

1.CLASS 1 LASER PRODUCT

2.DANGER : Invisible laser radiation when open and inter lock failed or defeated. Avoid direct exposure to beam.

3.CAUTION : There are no serviceable parts inside the Laser Unit. Do not disassemble the Laser Unit. Replace the complete Laser Unit if it malfunctions.

4.CAUTION : The compact disc player uses invisible laserradiation and is equipped with safety switches whichprevent emission of radiation when the drawer is open and the safety interlocks have failed or are de feated. It is dangerous to defeat the safety switches.

5.CAUTION : If safety switches malfunction, the laser is able to function.

6.CAUTION : Use of controls, adjustments or performance of procedures other than those specified herein may result in hazardous radiation exposure.

⚠ ***CAUTION*** **Please use enough caution not to see the beam directly or touch it in case of an adjustment or operation check.**

VARNING : Osynlig laserstrålning är denna del är öppnad och spårren är urkopplad. Betrakta ej strålen.

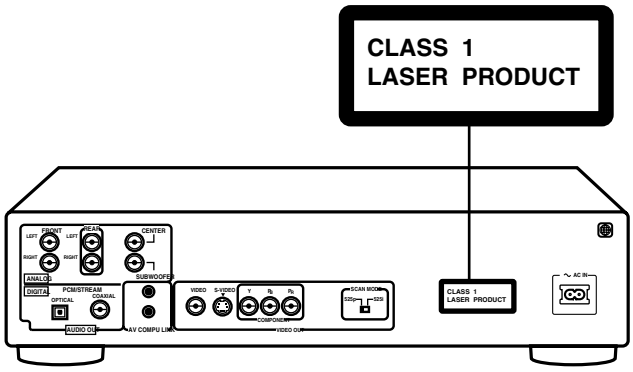
VARO : Avattaessa ja suojalukitus ohitettaessa olet alttiina näkymättömälle lasersäteilylle.Älä katso säteeseen.

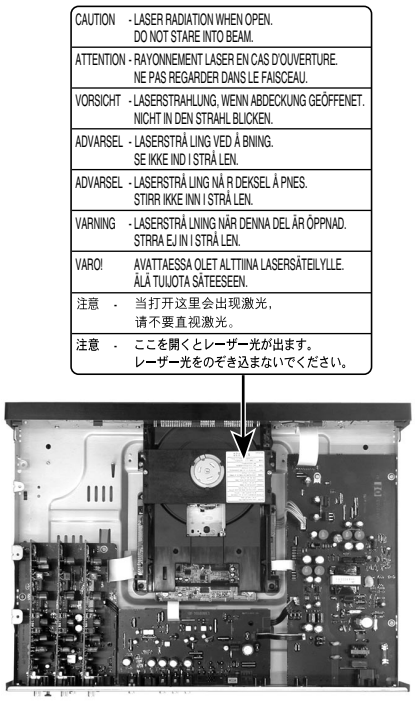
ADVARSEL : Usynlig laserstråling ved åbning , når sikkerhedsafbrydere er ude af funktion. Undgå udsættelse for stråling.

ADVARSEL : Usynlig laserstråling ved åpning,når sikkerhetsbryteren er avslott. unngå utsettelse for stråling.

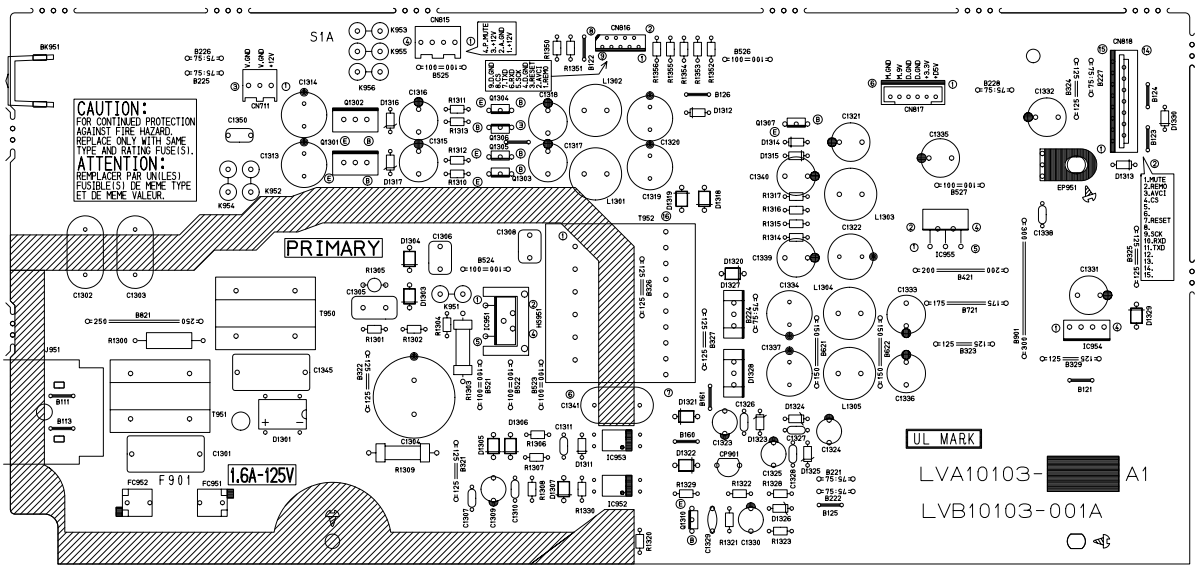
REPRODUCTION AND POSITION OF LABELS

WARNING LABEL





Importance Admistering point on the Safety



Note : It's means "J" for U.S.A. market model and "C" for canada market model.

XV-D721BK/XV-D723GD C/J ONLY	XV-721BK/XV-723GD C/J SEULEMENT
Full Fuse Replacement Marking Graphic symbol mark (This symbol means fast blow type fuse.) should be read as follows ;	**Marquage Pour Le Remplacement Complet De Fusible** Le symbole graphique (Ce symbole signifie fusible de type á fusion rapide.) doit être interprété comme suit ;
FUSE CAUTION	**PRECAUTIONS SUR LES FUSIBLES**
FOR CONTINUED PROTECTION AGAINST RISK OF FIRE, REPLACE ONLY WITH SAME TYPE AND RATING OF FUSES ; **F901 : 1.6 A / 125 V**	**POUR UNE PROTECTION CONTINUE CONTRE DES RISQUES D'INCENDIE, REMPLACER SEULEMENT PAR UN FUSIBLE DU MEME TYPE ;** **F901 : 1.6 A / 125 V**

Disassembly method

< Main body>

■Removing the top cover (See Fig.1)

1. Remove the four screws A on each side of the body.
2. Remove the two screws B on the back of the body.
3. Remove the top cover from behind in the direction of the arrow while pulling the lower part of the sides.

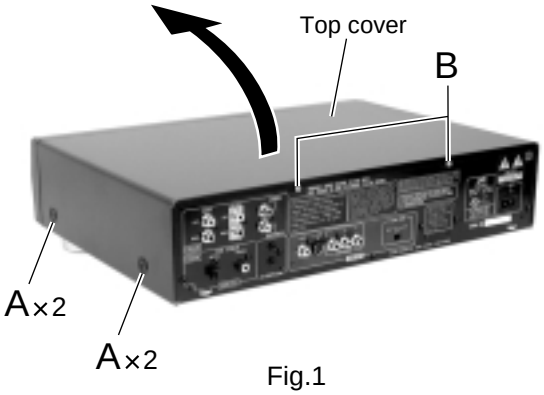


Fig.1

■Removing the rear panel (See Fig.2)

・Prior to performing the following procedure, remove the top cover.

1. Remove the sixteen screws C on the back of the body.

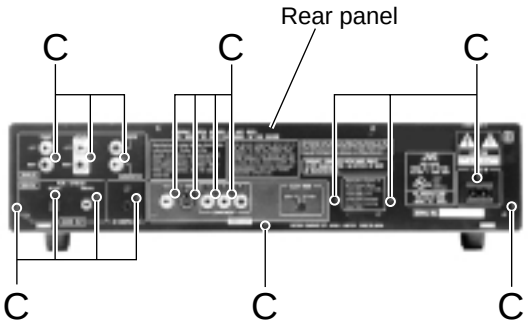


Fig.2

■Removing the fitting (See Fig.3 to 5)

・Prior to performing the following procedure, remove the top cover.

ATTENTION: To remove the front panel assembly and the DVD mechanism assembly, remove the fitting in advance.

1. Lower the mechanism by moving the lever marked a in the direction of the arrow from the upside of the body (Refer to Fig.3).
2. Manually eject the loading tray toward the front.
3. Remove the fitting from the loading tray by releasing the joints b on the both sides of the fitting.
4. Push and return the loading tray.

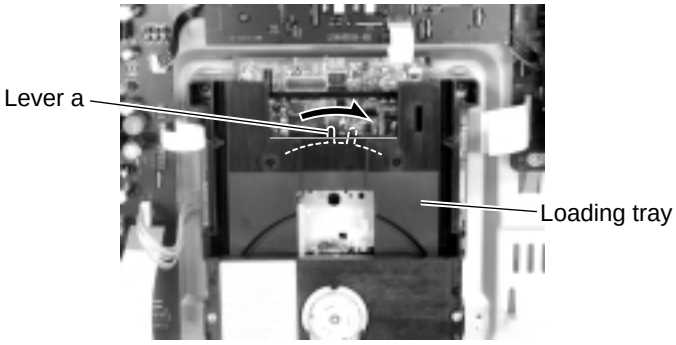


Fig.3

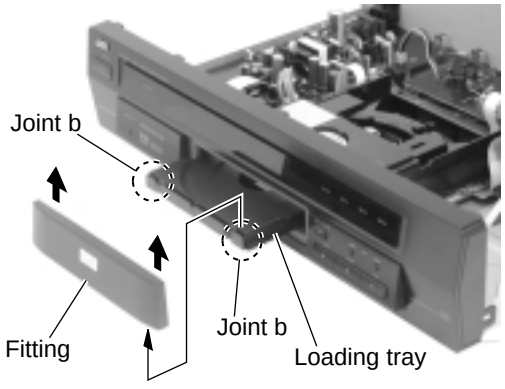


Fig.5

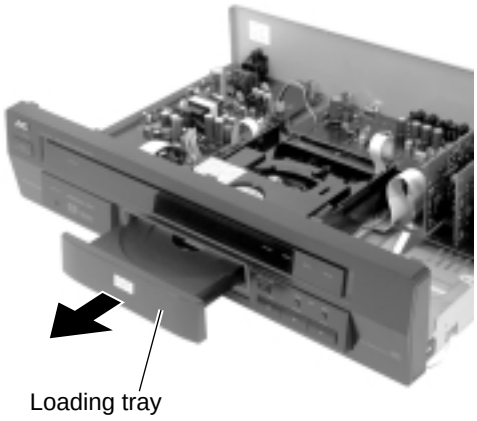


Fig.4

■Removing the front panel assembly (See Fig.6 to 9)

・Prior to performing the following procedure, remove the top cover and the fitting.

1. Disconnect the card wire from connector CN818 on the regulator board.

2. Turn back the body and remove the three screws D fixing the front panel assembly.

3. Release the two joints c on both sides of the body and remove the front panel assembly toward the front.

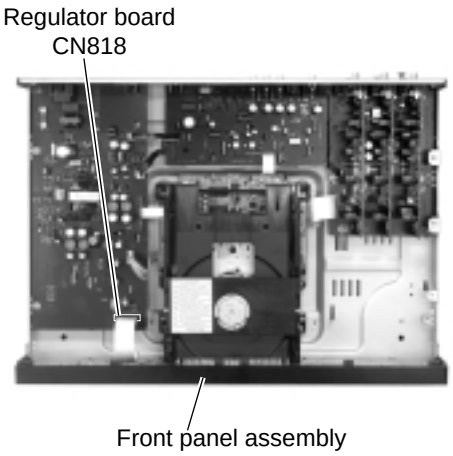


Fig.6

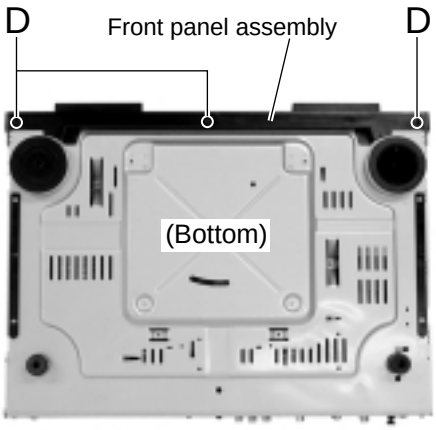


Fig.7

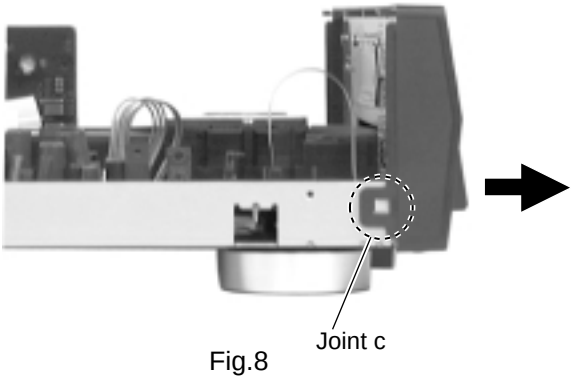


Fig.8

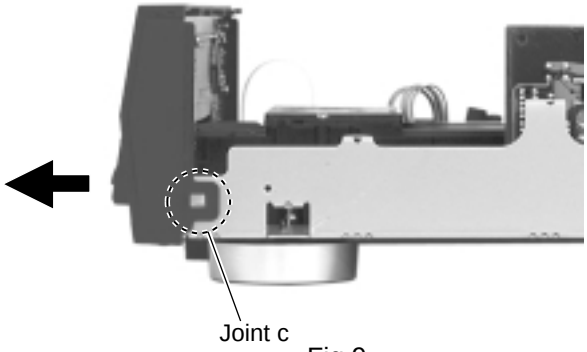


Fig.9

■Removing the DVD mechanism
(See Fig.10)

- Prior to performing the following procedure, remove the top cover and the fitting.
- It is not necessary to remove the front panel assembly.

1. Disconnect the card wire from connector CN816 and the harness from CN817 on the regulator board.
2. Disconnect the card wire from connector CN701 on the video board.
3. Disconnect the card wire from CN831 on the DSP board.
4. Remove the four screws E and the DVD mechanism assembly by pulling out from the front panel assembly backward.

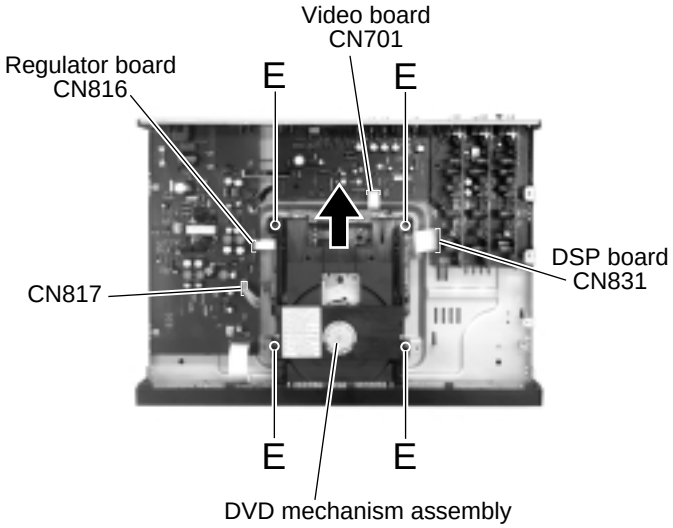


Fig.10

■Removing the regulator board
(See Fig.11 and 12)

- Prior to performing the following procedure, remove the top cover.
- It is not necessary to remove the rear panel.

1. Disconnect the card wire from connector CN816 and CN818 and the harnesses from CN815,CN817 and CN711 on the regulator board.
2. Remove the three screws F attaching the regulator board.
3. Remove the two screws C on the rear panel.

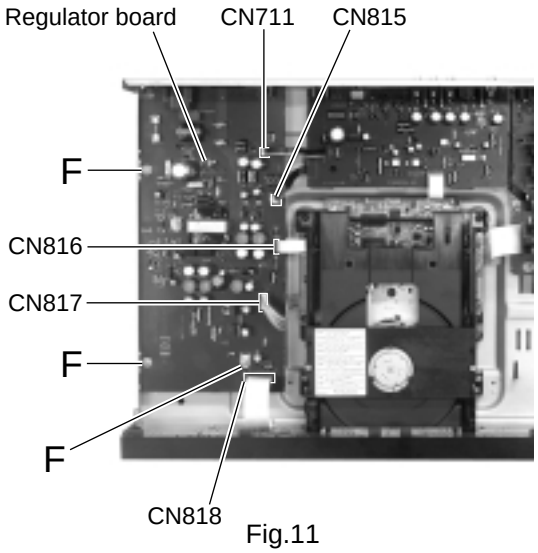


Fig.11

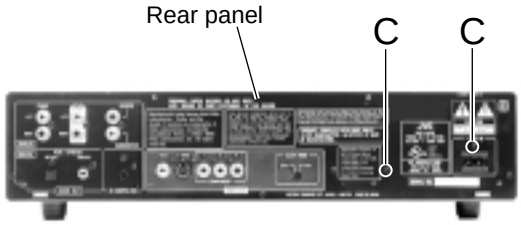


Fig.12

■Removing the video board (See Fig.13 and 14)

・Prior to performing the following procedure, remove the top cover.

Ref. : It is not necessary to remove the rear panel.

1. Disconnect the harnesses from the connector CN711 on the regulator board.
2. Disconnect the card wire from connector CN701 on the video board.
3. Remove the five screws C on the rear panel.

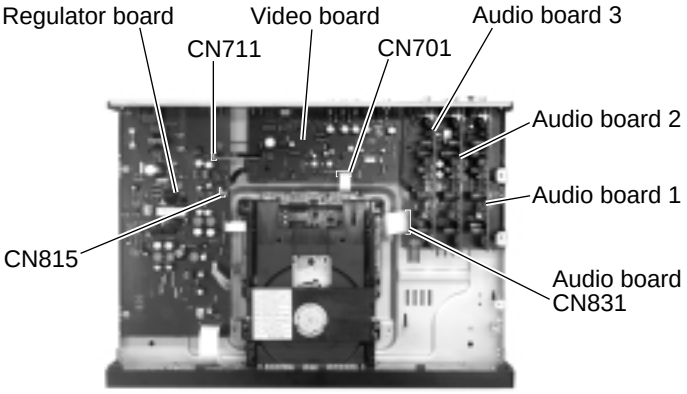


Fig.13

■Removing the Audio board 1,2 and 3 / the Audio board (See Fig.13,15 and 16)

・Prior to performing the following procedure, remove the top cover and rear panel.

1. Remove the three screws C attaching the audio board 1,2 and 3.
2. Disconnect the audio board 1,2 and 3 from the audio board respectively.
3. Disconnect the harnesses from connector CN815 on the regulator board.
4. Disconnect the card wire from connector CN831 on the audio board.
5. Remove the two screws G attaching the audio board.

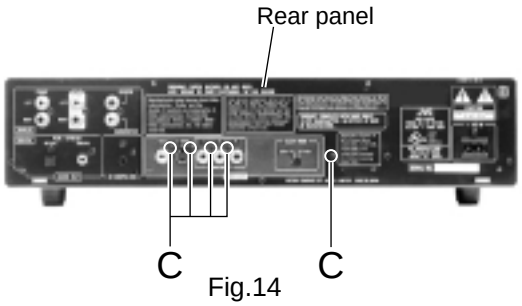


Fig.14

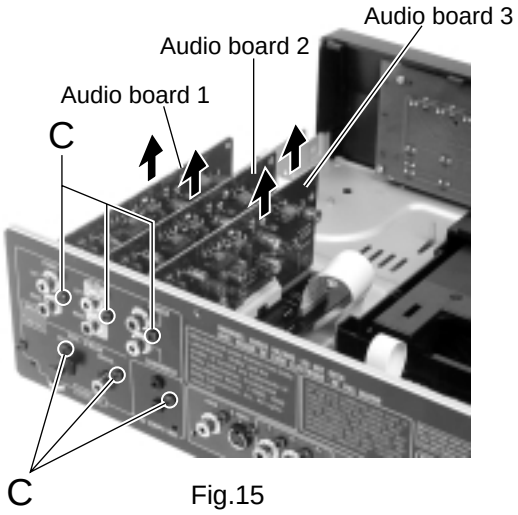


Fig.15

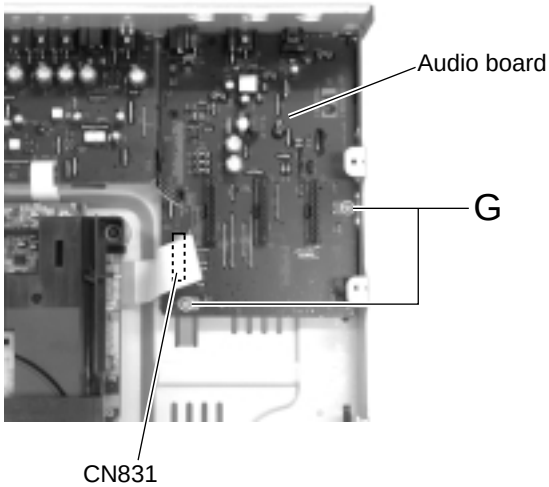


Fig.16

■Removing the DVD servo board (See Fig.17)

・Prior to performing the following procedure, remove the top cover and the DVD mechanism assembly.

1. Turn over the DVD mechanism assembly and disconnect the card wire from connector CN102 and CN103 on the DVD servo board.

2. Remove the two screws H attaching the DVD servo board. Move the DVD servo board in the direction of the arrow to release the two corner joints d.

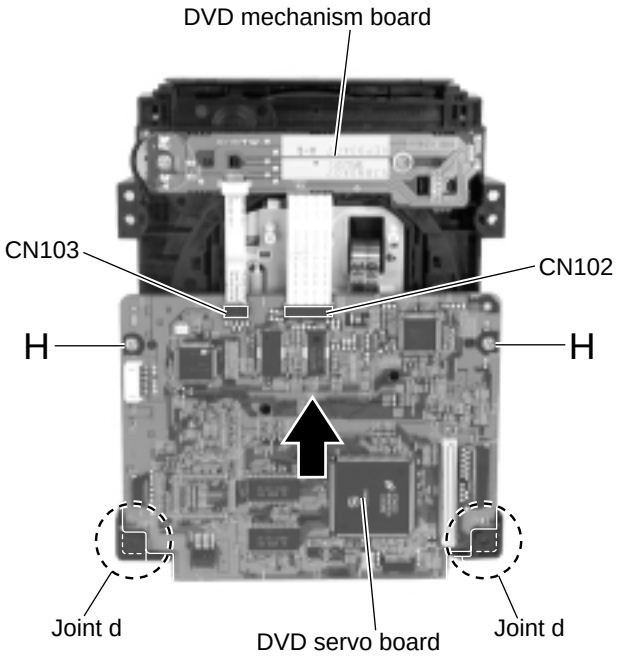


Fig.17

<Front panel assembly>

・Prior to performing the following procedure, remove the top cover and the front panel assembly.

■Removing the FL board / the power switch board (See Fig.18 and 19)

1. Remove the eight screws I and three screws J on the back of the front panel assembly. Remove the FL board and the power switch board at the same time.

2. Disconnect the harness from connector CN903 on the FL board.

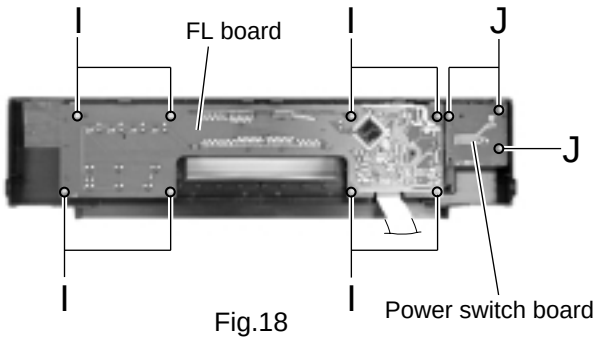


Fig.18

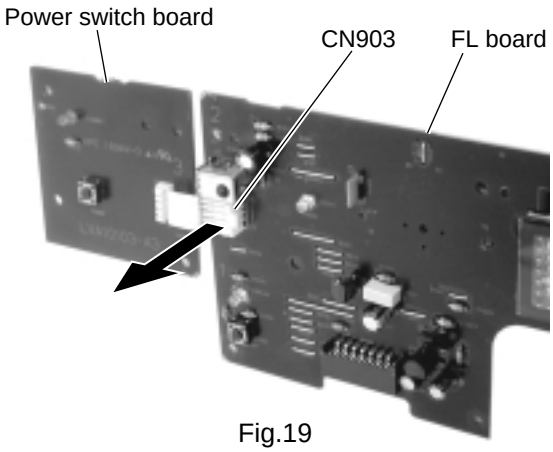


Fig.19

Adjustment method

This model has the TEST mode for simple diagnosis of the internal function. Use the TEST mode for diagnosing and checking the set as mentioned below.

■ **Details of the TEST mode**

The TEST mode comprises the five modes of the following.

FL indication (*: numeral)

1.DVD AUDIO copyright protection key serial indication ---------- ********
Indicates the content of the DVD AUDIO copyright at shipment. Use this mode for checking it.

2.Microcomputer's version number indication ---------- **_**_**
Indicates the initial version number of the microcomputer at shipment. Use this mode for checking it.

3.Servo signal system check mode ---------- CHECK
Use this mode for checking the laser pickup status.

4.Indication check mode ---------- The FL and LED's go on in full.
The LED's and FL of the set go on in full. Use this mode for checking indications.

5.Microcomputer software upgrading mode ---------- UPGRADE
Use this mode for upgrading the microcomputer software.

■ **How to set the TEST mode**

1.While pressing the STOP key and PLAY key of the set together, plug in the power cord.
*Continue to pressing both the STOP key and PLAY key until reading of disk data completes (until the "NOW READING" message changes into a DVD logo).

2."TEST *" message appears on the FL. (* In the part of the sign, the sign is different according to the destination.)

3.The five modes of the TEST mode change one after another each time the DISPLAY OFF key of the set is pressed.

4.To recover the usual operation mode, turn off the set by pressing the POWER ON/OFF key.

■ **How to check the laser pickup**

Since the laser pickup of the set is easily affected by static electricity, heat, etc., it may be damaged depending on use condition. If the set shows such a symptom as it fails in reading disk data, check the laser pickup as follows.

* Checking laser current

1.Enter the set into the "servo signal system check mode" of the TEST mode.

2.Press the SKIP |◀◀ key of the set.
The laser is turned on and the LAS **** message appears on the FL display. **** in the message indicates the current in code. For knowing the actual laser current, read the first two figures (omitting the last two figures) and convert the number into the current (mA) referring to the following conversion table, because the FL indication is a hexadecimal number. Since the FL indication varies because of self-heating of the set, read the indication value about 20 seconds after the set was turned on. If the indicated value is the OK level (see the conversion table), the laser is judged to be normal in the initial status by this simple checking method.

3. Press the STOP key to set back the check mode to the initial status.

Laser current conversion table

FL indication	Current (mA)	Judgment	FL indication	Current (mA)	Judgment	FL indication	Current (mA)	Judgment
38	1.2	OK	04	35.6	OK	D0	70.0	NG
34	3.9	OK	00	38.3	OK	CC	72.7	NG
30	6.5	OK	FC	40.9	OK	C8	75.3	NG
2C	9.1	OK	F8	43.6	OK	C4	78.0	NG
28	11.8	OK	F4	46.2	OK	C0	80.0	NG
24	14.4	OK	F0	48.8	OK	BC	83.2	NG
20	17.1	OK	EC	51.5	OK	B8	86.0	NG
1C	19.7	OK	E8	54.1	OK	B4	88.5	NG
18	22.4	OK	E4	56.8	OK	B0	91.2	NG
14	25.0	OK	E0	59.4	OK	AC	93.8	NG
10	27.7	OK	DC	62.1	NG	A8	96.5	NG
0C	30.3	OK	D8	64.7	NG	A4	99.1	NG
08	33.0	OK	D4	67.4	NG			

* Automatic adjustment/Jitter value indication

1.Enter the set into the "servo signal system check mode" of the TEST mode.
2.Open the tray with the OPEN key of the set. Set the TEST disk VT-501 on the tray and put back the tray with the CLOSE key. Then, press the PAUSE key.
The TEST disk starts rotation to execute automatic adjustment. If the set is in the normal condition, the "CHECK OK" message appears. If there is something abnormal in the adjustment values, an error message appears and it mostly comes from a failure in the servo system (including the mechanism and pickup). In such the event, refer to the check points by errors.
When using the TEST disk VT-501, carefully check to see if there is neither damage nor dirt on the read surface of the disk beforehand.
3.Press the STOP key to return the check mode to the initial status.
4.After the automatic adjustment with the TEST disk completes, press the PLAY key.
The disk starts rotation and a jitter value (signal read precision in percentage) appears on the FL display (JIT 0***). If the indication value (in *** places) is 110 (11 %) or less, it can be judged by this simple checking method that the signal read precision of the set is satisfactory.
Before using the TEST disk VT-501, carefully check it if there is neither damage nor dirt on the read surface.
5.Press the STOP key to return the mode to the initial status.

■ Upgrading microcomputer software

The internally incorporated microcomputer software of this set can be revised in part for the reason that the set is designed to conform to new standards and to be capable of playing disks to be put on the market by other manufacturers. To upgrade the internal microcomputer software, use the upgrade disk and follow the procedure mentioned below.

* How to upgrade the microcomputer software

1.Set the upgrade disk in the set and enter it into the TEST mode.
2.After confirming that the set completes reading of the upgrade disk data while looking at the indication on the monitor screen, change the TEST mode to the microcomputer software upgrading mode and then press the PLAY key.
3.The set completes writing of the upgrade disk data approximately 1 minute later and it is automatically reset by the self-resetting function. Then the set again reads the upgrade disk and stops automatically.
4.Take the upgrade disk out of the set and turn it off with the POWER ON/OFF key.
5.Again enter the set into the TEST mode, and press the SKIP ▶▶| key and then the PAUSE key.
6.Make sure that the DVD AUDIO indicator goes on a few seconds after the above-mentioned operation, check the version number of the microcomputer software in the microcomputer software version number indication mode.
*Carefully carry out the above procedure. If data write is interrupted in the middle of course by power failure or careless shutdown operation, not only the data of the internal software may be damaged but the set may fail in resetting. The version number of the internal microcomputer software is shown as follows.

FL indication: ** ** **
[IC901] [IC401] [IC508/IC509] ↵ Symbol number of microcomputer IC

■ Initializing the set

Initialization of the set returns it to the initial status at shipment.
Be sure to initialize the set after repair service.

* How to initialize the set

1.Enter the set into the TEST mode and press the SKIP ▶▶| key first and the PAUSE key second.
2.Make sure that the DVD AUDIO indicator goes on a few seconds later.

■ DVD AUDIO copyright protection

To protect the DVD AUDIO copyright from infringement, a number proper to each DVD AUDIO set called a device key is assigned to each set. If a proper device key is not set for a set, it fails in playing a copyrighted disk.
The management number of the device key of a set can be checked by the DVD AUDIO copyright protection key serial indication in the TEST mode. If the "???...." message appears in this check mode, the set has a failure in the device key. If it occurs, inquire at the Service Section of the Audio and Communication Division, JVC.

Check points for each error

(1) Spindle start error

*Defective spindle motor
Are there 10ohms resistance between each pin of CN102 "1~4"?
(The power supply is turned off and measured.)

*Hall element: Is sine wave output between CN102 "10" and "11", between "12" and "13", and between "14" and "15" during rotation?

In either case, replace the mechanical unit.

*Defective spindle driver (IC251)
Is a driving wave output from CN102 "1~4" ?

During rotation 

Is IC251 "9" at "H" level (START)?
Servo IC --- Is control signal sent to the motor driver ?

IC201 "95" : Duty is 50% during stop, but varies during rotation (greatly varies at start).
--- If not sent, pattern or servo IC (IC201) is defective.

R259 : approx 2.5V during stop, but varies during rotation (greatly varies at start).
--- of not sent, pattern or servo IC (IC201) is defective.

Is FG input to servo IC ?
Observe FG wave from IC201 "89". --- If not output, pattern, IC251 or IC201 is defective.

(2) Disc Detection, Distinction error (no disc, no REFNV)

* Laser is defective.
* Front End Processor is defective (IC101).
* APC circuit is defective. --- Q101.
* Pattern is defective. --- Lines for CN101 "15" and "17".
Lines for between IC201 "2" and IC101 "2"(LDONA),
between IC201 "3" and IC101 "1" (LDONB).
* Servo IC is defective (IC201).
* Is signal sent to IC201(servo)"71" AS2 ?
* IC101 --- For signal from IC101 to IC301, is signal output from IC101 "88" (RFAS1) and IC101 "69" REENV ?

(3) Traverse movement NG

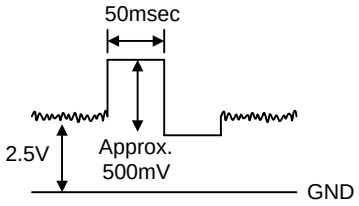
* For automatic adjustment, traverse movement occurs only when the position is changed to retry judging the disc type after the 1st judgment resulted in an error. Therefore, traverse movement rarely occurs because, in most cases, disc judgment at the current position (1st time judgment) is executed successfully. (Of course, NG rarely occurs in this step.)

Note: 1st time judgment of disc type resulted in NG. --- The re-judgment of disc type may not be successful. Therefore, after removing the cause of traverse movement, re-execute automatic adjustment and confirm that no problem exists.

* Check point

a) During stop
Whether 50% duty pulse is output to R273
Whether between R274 and C271 is at approx. 2.5VDC
Offset voltage between CN102 "1" and "2" (scores mV if exists)

b) When tray is opened or closed
Check by oscilloscope whether a rectangular wave signal is output from CN102 "1" or "2".



If checking a) or b) resulted in NG, IC201 maybe defective.

(4) Focus ON NG

* Is FE output ? --- Pattern, IC101
* Is FCDRV signal sent ? (R286) --- Pattern, IC301
* Is driving voltage sent ?
CN101 "1", "3" --- If NG, pattern, driver, mechanical unit (with the power turned off, measure the resistance between CN101 "20" and "21").
* Does CN101 "8" become "H" and is the focus drawing in done?
--- Mechanical unit (laser power too low), IC101(defective gain)
--- Moreover, It is thought that abnormality is found in the disk.
* Mechanical unit is defective.

(5) Tracking ON NG

* When the tracking loop cannot be drawn in, IC201 "58" (/TRON) does not become "L".
* Mechanical unit is defective.
Because the undermentioned adjustment value is abnormal, it is not possible to draw in normally.
* Periphery of driver (IC271)
Constant or IC it self is defective.
(When passing without becoming abnormal while adjusting the following.)
* Servo IC (IC201)
When improperly adjusted due to defective IC.

[Focus position rough adjustment]
[Phase difference cancellation rough adjustment]
[Tracking balance adjustment]

(6) Spindle CLV NG

* When the spindle cannot be shifted to CLV Servo, does not become "H" between IC201 "18" and IC301"88".
* IC201 Is signal output from IC101 "87" (RFOP)?
* IC201 Is signal output from IC201 "60" to "64" (binary-coded clock and data)?
* IC201 Is "58" (/TRON) at "L" level ?
* IC301 "74" to "76" --- Is signal output to IC201 "24", "25", "28" (In case of only CD). (Serial communication of rotation information)
* Spindle motor driver is defective.
  Even when one of the three phases is defective, item (1) may be passed.
  --- Check the second item in (1) above.
* C260 to C263 Defective soldering
  If noise eliminating capacitors are not properly soldered, noise may ride on the waveform.
* Besides, the undermentioned cause is thought though specific of the cause is difficult because various factors are thought.
  Mechanism is defective.(jitter)
  IC101, IC201.

(7) Address read NG

* Besides, the undermentioned cause is thought though specific of the cause is difficult because various factors are thought.
  Mechanism is defective. (jitter)
  IC201, IC301, IC401.
  The disc is dirty or the wound has adhered.

(8) Between layers jump NG (double-layer disc only)

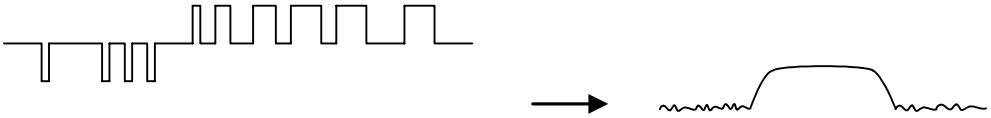
* When the focus flight is generated when jumps between layers.
  Because all adjustments for L1 layer must be successful, this error may rarely be due to a circuit defect.
* Crosstalk might occur from tracking to focus system. (See (11)) --- Replace the mechanical unit.
* Driver surroundings.
* Defect of constant and IC.
* For double-layer discs, after checking CLV on layer L1, jumps to layer L0 after mode changes to FG. Then tracking is turned off, and adjustments are executed from the focus position coarse adjustment in order.
* When the jump between layers is done on the single-layer disk, the disk distinction error is thought.
  --- The laser power is low (RF level is confirmed by IC101"87" (RFOP)).
  --- AS1, AS2, REFNV Is the signal sent to between IC101 and IC201 ?

(9) Neither picture nor sound is output

* Cannot search

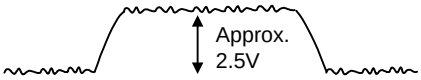
a) Can the feed system be driven?

Check the waveform of TRSDRV signal (R273). --- Waveform between R274 and C271.



Search results in a change of duty
(three values with 2.5V at the center)
(The figure is exaggerated.)

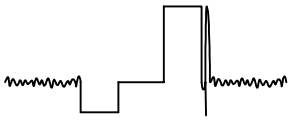
Check the waveform of CN101 "1" and "2". --- After the driver (IC271)



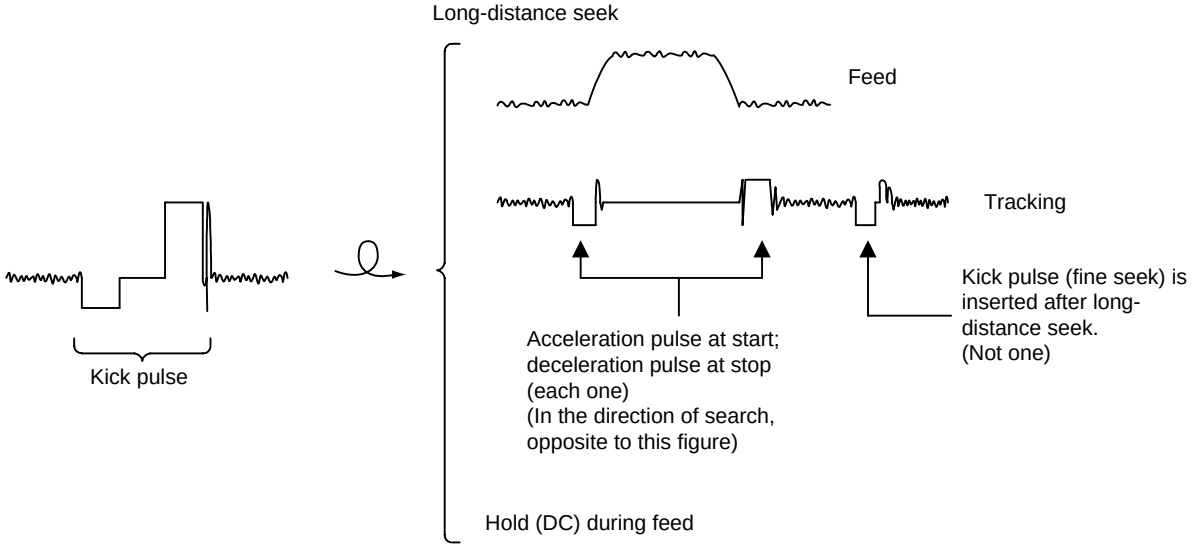
For short-distance search, the waveform becomes roundish, not trapezoidal, and voltage is low.

b) Is kick available?

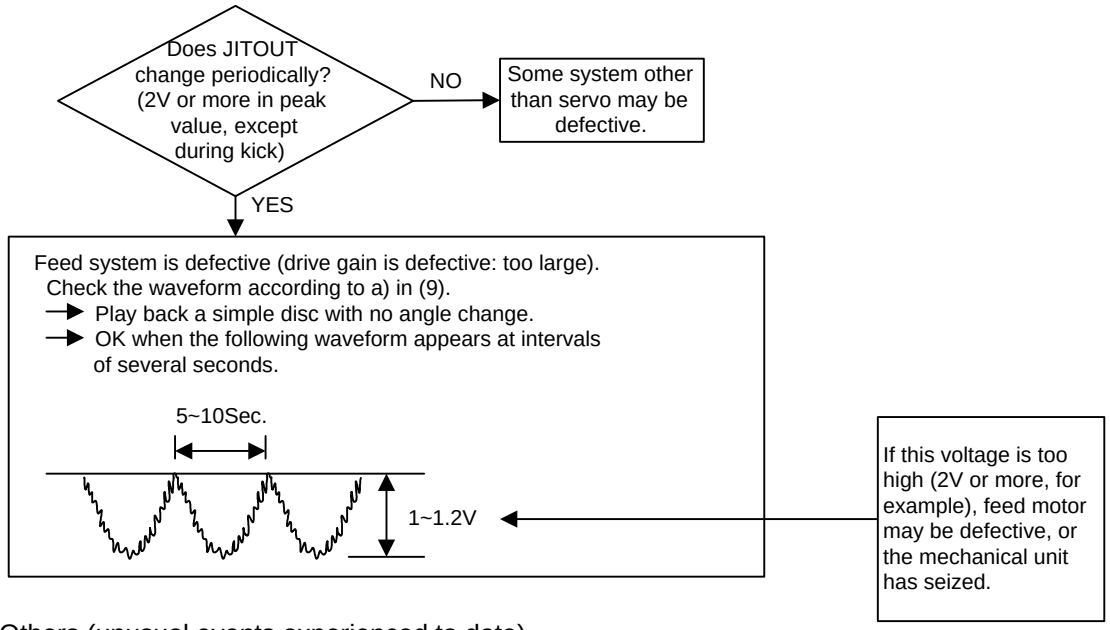
Check the TRDRV signal waveform from R289.



Check the waveform of CN101 "2" and "4" --- After the driver (IC271)
Although differs in amplitude and DC offset, the waveform is similar to that of R289



(10) Picture is distorted or abnormal sound occurs at intervals of several seconds.



(11) Others (unusual events experienced to date)

* Problem occurs with double-layer discs although no problem occurs with single-layer DVD.
(Error occurs, or search becomes unstable and takes longer.)
Crosstalk might occur from tracking to focus system.
--- When FE was observed during search (skip, etc.), it was found that a wave resembling TE with an amplitude of 200mVp-p was riding on FE.
--- Mechanical unit was replaced.

* Error frequently occurred in the outer part of discs although no error occurred in the inner part.
--- Mechanical unit was replaced because tilt seemed to be defective.

(12) CD During normal playback operation

a) Is TOC reading normal? —NO→ Please refer to "Servo Volume" flow.
Displays total time for CD-DA.
Shifts to double-speed mode for V-CD.
↓ YES
b)Playback possible? —NO→ *--:-- is displayed during FL serch.
According to [*Cannot serch] for DVD(9), check the feed and tracking systems.
*No sound is output although the time is displayed.(CA-DA)
*DAC, etc, other than servo.
*The passage of time is not stable, or picture is abnormal.(V-CD)
*The wound of the disc and dirt are confirmed.

(13) Others

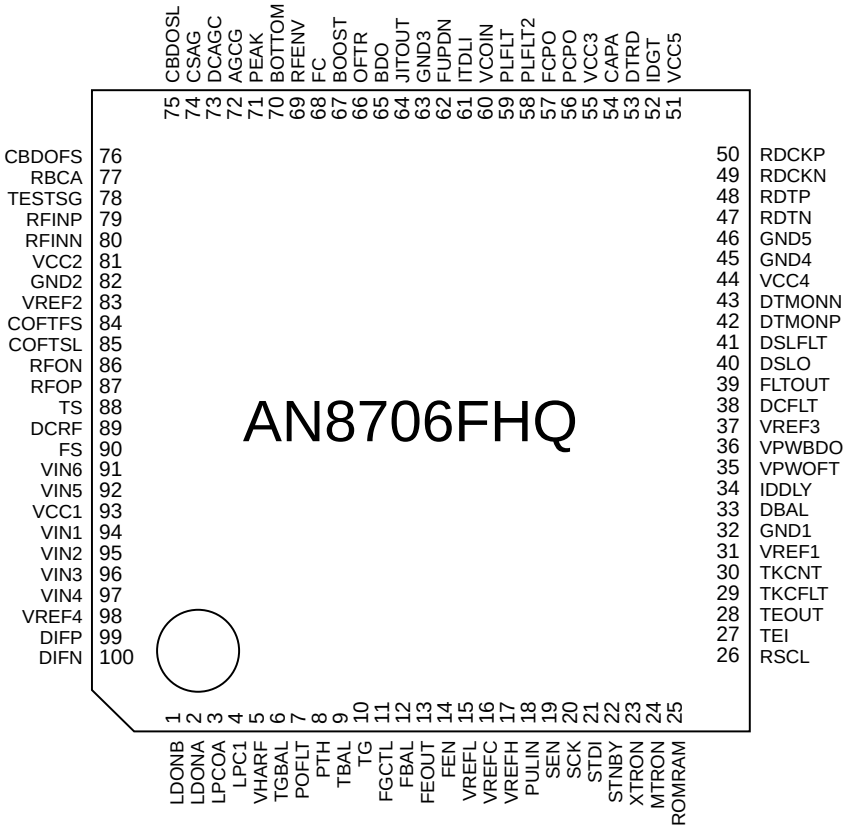
V-CD : Frequent occurrence of error in inside and outer.
(Even the disk without the wound : when generated.)

Waveform observation
--- Is the oscillation frequency of about 700~900Hz output?
(Borrow a pertinent disk for the complaint for the combination with the disk.)
--- Exchanges mechanism for the mechanism resonance.

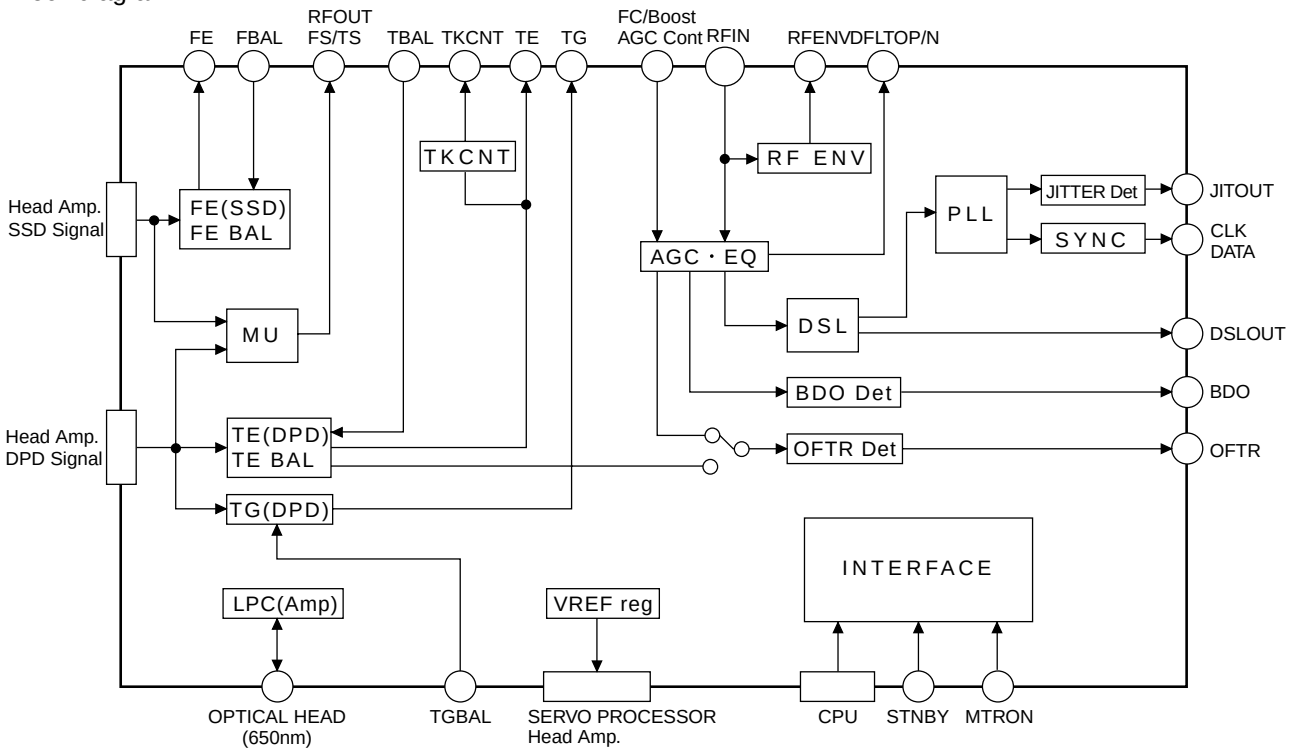
Description of major ICs

■ AN8706FHQ (IC101) : Front end processor

1.Pin layout



2.Block diagram



3.Pin function

AN8706FHQ (1/2)

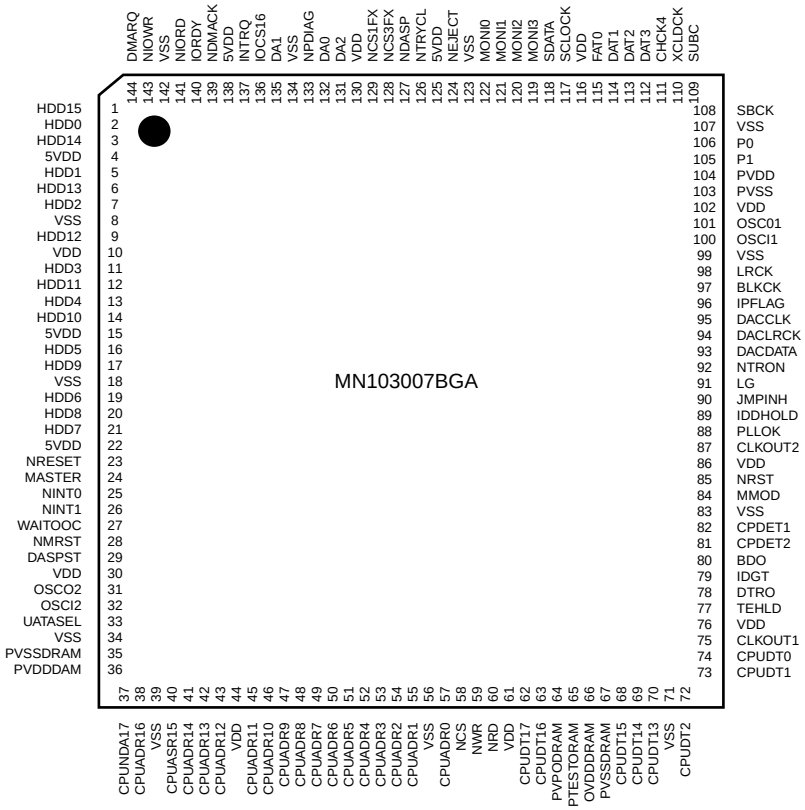
Pin No.	Symbol	I/O	Functions
1	LDONB	I	Laser ON (CD Head) terminal
2	LDONA	I	Laser ON (DVD Head) terminal
3	LPCOA	O	Laser drive output terminal
4	LPC1	I	Laser PIN input terminal
5	VHARF	O	VHALF voltage output terminal
6	TGBAL	I	Tangential phase balance control terminal
7	POFLT	O	Track detection Threshold value level terminal
8	PTH	I	Track detection Threshold value level terminal
9	TBAL	I	Tracking balance control terminal
10	TG	O	Tangential phase error signal output terminal
11	FGCTL	I	Focus amplifier Gain control terminal
12	FBAL	I	Focus balance control terminal
13	FEOUT	O	Focus error signal output terminal
14	FEN	I	Focus error output amplifier reversing input terminal
15	VREFL	O	VREFL voltage output terminal
16	VREFC	O	VREFC voltage output terminal
17	VREFH	O	VREFH voltage output terminal
18	PULIN	I	DSL,PLL drawing mode switch terminal
19	SEN	I	SEN(Cereal data input terminal)
20	SCK	I	SCK(Cereal data input terminal)
21	STDI	I	STDI(Cereal data input terminal)
22	STNBY	I	Standby mode control terminal
23	XTRON	I	Tracking OFF holding input terminal
24	MTRON	I	Monitor output ON/OFF switch terminal
25	ROMRAM	I	ROM･RAM switch terminal
26	RSCL	O	Standard current source terminal
27	TEI	I	Tracking error output Amp reversing input terminal
28	TEOUT	O	Tracking error signal output terminal
29	TKCFLT	O	Track count detection filter terminal
30	TKCNT	O	Track count output terminal
31	VREF1	O	VREF1 voltage output terminal
32	GND1	O	Earth terminal 1
33	DBAL	I	Data slice offset adjustment terminal
34	IDDLY	I	Data slice delay adjustment terminal
35	VPWOFT	I	OFTR detection level setting terminal
36	VPWBDO	I	BDO detection level setting terminal
37	VREF3	O	VREF3 voltage output terminal
38	DCFLT	O	Capacity connection terminal for data slice input filter
39	FLTOUT	O	Filter amplifier output terminal
40	DSLO	O	Data slice single data output terminal
41	DSLFLT	O	Constant filter terminal when data is sliceddelly
42	DTMONP	O	PLL differential motion 2 making to value edge signal moniter output (+)
43	DTMONN	O	PLL differential motion 2 making to value edge signal moniter output (-)
44	VCC4	I	Power terminal 4 (5V)
45	GND4	O	Earth terminal 4
46	GND5	O	Earth terminal 5
47	RDTN	O	PLL differential motion making to synchronization RF signal reversing output
48	RDTP	O	PLL differential motion making to synchronization RF signal rotation output
49	RDCKN	O	PLL differential motion making synchronization clock reversing output
50	RDCKP	O	PLL differential motion making synchronization clock rotation output

AN8706FHQ(2/2)

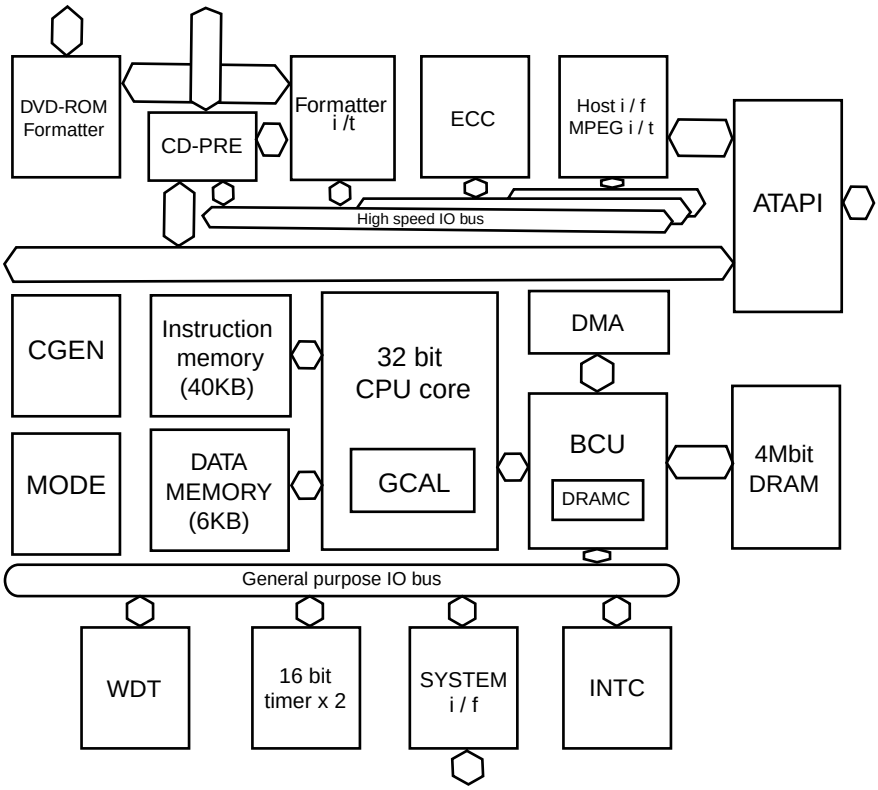
Pin No.	Symbol	I/O	Functions
51	VCC5	I	Power terminal 5 (3.3V)
52	IDGT	I	Data slice part address part gate signal input terminal (For RAM)
53	DTRD	I	Data slice data read signal input terminal(For RAM)
54	CAPA	I	Data slice CAPA(Address)signal input terminal (For RAM)
55	VCC3	I	Power terminal 3 (5V)
56	PCPO	O	PLL phase gain set terminal
57	FCPO	O	PLL frequency gain set terminal
58	PLFLT2	O	PLL low region filter terminal
59	PLFLT	O	PLL high region filter terminal
60	VCOIN	I	PLL VCO input terminal
61	ITDLI	O	PLL jitter free current ripple removal filter terminal
62	FUPDN	I	PLL frequency control input terminal
63	GND3	O	Earth terminal 3
64	JITOUT	O	Detection signal output of jitter
65	BDO	O	BDO output terminal
66	OFTR	O	OFTR output terminal
67	BOOST	I	Booth control terminal for filter
68	FC	I	FC control terminal for filter
69	RFENV	O	RF enve output terminal
70	BOTTOM	O	Bottom enve detection filter terminal
71	PEAK	O	Peak enve detection filter terminal
72	AGCG	O	AGC amplifier gain control terminal
73	DCAGC	O	AGC amp filter terminal
74	CSAG	O	Sag cancellation circuit filter terminal
75	CBDOSL	O	BDO detection capacitor terminal
76	CBDOFS	O	BDO detection capacitor terminal
77	RBCA	O	BCA detection level setting terminal
78	TESTSG	I	TEST signal input terminal
79	RFINP	I	RF signal positive moving input terminal
80	RFINN	I	RF signal reversing input terminal
81	VCC2	I	Power terminal 2 (5V)
82	GND2	O	Earth terminal 2
83	VREF2	O	VREF2 voltage output terminal
84	COFTFS	O	OFTR detection capacitor terminal
85	COFTFL	O	OFTR detection capacitor terminal
86	RFON	O	RF signal output terminal P
87	RFOP	O	RF signal output terminal N
88	TS	O	All addition amplifier (DVD) output terminal
89	DCRF	O	All addition amplifier capacitor terminal
90	FS	O	All addition amplifier (CD) output terminal
91	VIN6	I	Focus input of external division into two terminal
92	VIN5	I	Focus input of external division into two terminal
93	VCC1	I	Power terminal 1 (5V)
94	VIN1	I	External division into four (DVD/CD) RF input terminal 1
95	VIN2	I	External division into four (DVD/CD) RF input terminal 2
96	VIN3	I	External division into four (DVD/CD) RF input terminal 3
97	VIN4	I	External division into four (DVD/CD) RF input terminal 4
98	VREF4	O	VREF4 voltage output terminal
99	DIFP	O	RF signal (RAM) output terminal P
100	DIFN	O	RF signal (RAM) output terminal N

MN103007BGA (IC301) : Optical disc controller

1.Terminal layout



2.Block diagram



3.Function

MN103007BGA(1/2)

Pin NO.	Symbol	I/O	Function
1	HDD15	I/O	ATAPI data
2	HDD0	I/O	ATAPI data
3	HDD14	I/O	ATAPI data
4	5VDD		
5	HDD1	I/O	ATAPI data
6	HDD13	I/O	ATAPI data
7	HDD2	I/O	ATAPI data
8	VSS		
9	HDD12	I/O	ATAPI data
10	VDD		
11	HDD3	I/O	ATAPI data
12	HDD11	I/O	ATAPI data
13	HDD4	I/O	ATAPI data
14	HDD10	I/O	ATAPI data
15	5VDD		
16	HDD5	I/O	ATAPI data
17	HDD9	I/O	ATAPI data
18	VSS		
19	HDD6	I/O	ATAPI data
20	HDD8	I/O	ATAPI data
21	HDD7	I/O	ATAPI data
22	5VDD		
23	NRESET	I	ATAPI reset
24	MASTER	I/O	ATAPI master / slave selection
25	NINT0	O	System control interruption 0
26	NINT1	O	System control interruption 1
27	WAITODC	O	System control weight control
28	NMRST	O	System control reset
29	DASPST	I	DASP signal initializing
30	VDD		
31	OSCO2	I,O	VSS connection,OPEN
32	OSCI2	I,O	VSS connection, OPEN
33	UATASEL	I	VSS connection
34	VSS		
35	PVSSDRAM		
36	PVDODRAM		
37	CPUADR17	I	System control address
38	CPUADR18	I	System control address
39	VSS		
40	CPUADR15	I	System control address
41	CPUADR14	I	System control address
42	CPUADR13	I	System control address
43	CPUADR12	I	System control address
44	VDD		System control address
45	CPUADR11	I	System control address
46	CPUADR10	I	System control address
47	CPUADR9	I	System control address
48	CPUADR8	I	System control address
49	CPUADR7	I	System control address
50	CPUADR6	I	System control address
51	CPUADR5	I	System control address
52	CPUADR4	I	System control address
53	CPUADR3	I	System control address
54	CPUADR2	I	System control address
55	CPUADR1	I	System control address
56	VSS		GND
57	CPUADR0	I	System control address
58	NCS	I	System control chip selection
59	NWR	I	System control wright
60	NRD	I	System control lead
61	VDD		Apply 3V
62	CPUDT7		System control data
63	CPUDT6		System control data
64	PVPPDRAM	O	C=10000PF is connected between VSS
65	PTESTDRAM	I	VSS connected
66	OVDDDRAM		
67	PVSSDRAM		
68	CPUDT5		System control data
69	CPUDT4		System control data
70	CPUDT3		System control data
71	VSS		GND
72	CPUDT2		System control data
73	CPUDT1	I/O	System control data
74	CPUDT0	I/O	System control data
75	CLKOUT1	O	16.9/11.2/8.45MHz clock
76	VDD	-	Apply 3V
77	TEHLD	O	Mirror gate
78	DTRO	O	Data part frequency control switch
79	IDGT	O	Part CAPA switch
80	BDO	I	RF dropout / BCA data of making to binary
81	CPDET2	I	Outer side CAPA detection
82	CPDET1	I	Side of surroundings on inside
83	VSS		GND
84	MMOD	I	VSS connected
85	NRST	I	System reset
86	VDD	-	Apply 3V
87	CLKOUT2	O	16.9MHz clock
88	PLLOK	O	Frame mark detection
89	IDOHOLD	O	ID gate for tracking holding
90	JMPINH	O	Jump prohibition

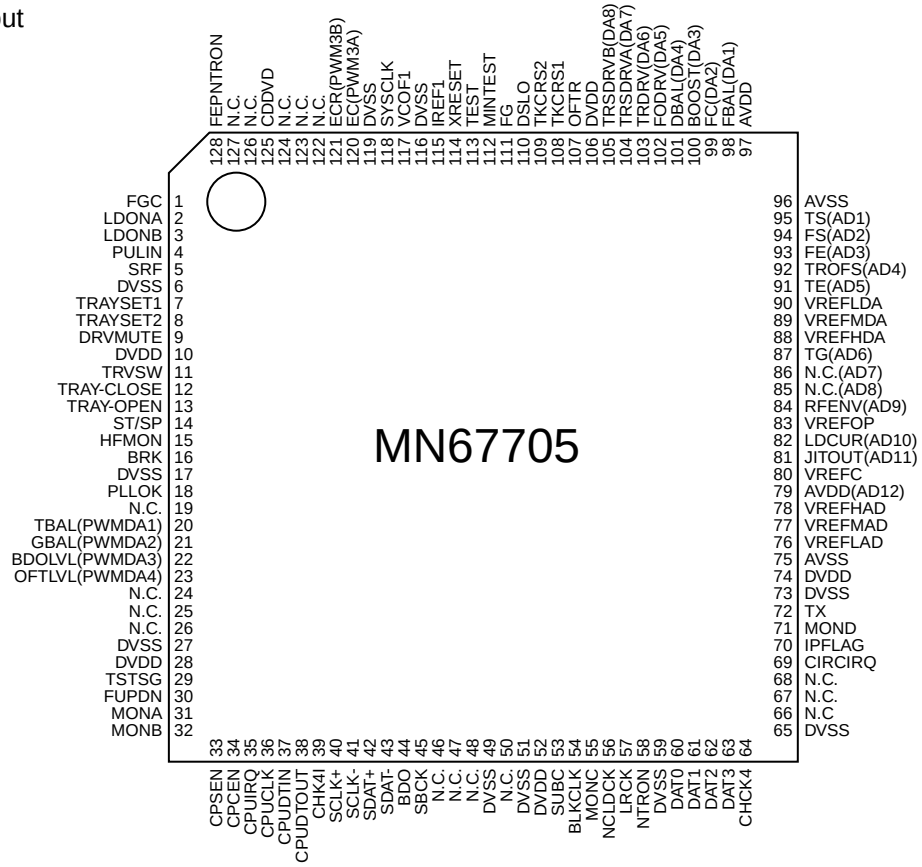
MN103007BGA(2/2)

Pin NO.	Symbol	I/O	Function
91	LG	O	Land / group switch
92	NTRON	I	Tracking ON
93	DACDATA	O	Cereal output
94	DACLRCK	O	L and R identification output
95	DACCLK	I	Clock for cereal output
96	IPFLAG	I	Interpolation flag input
97	BLKCK	I	Sub-code,Block clock input
98	LRCK	I	L and R identification signal output
99	VSS		
100	OSCI1	I,O	16.9MHz oscillation
101	OSCO1	I,O	16.9MHz oscillation
102	VDD		
103	PVSS		
104	PVDD		
105	P1	I/O	Terminal MASTER polarity switch input
106	P0	I/O	CIRC-RAM OVER/UNDER Interruption signal input
107	VSS		
108	SBCK	O	Sub-code, Clock output for serial input
109	SUBC	I	Sub-code, Cereal input
110	XCLDCK	I	Sub-code, Frame clock input
111	CHCK4	I	Read clock to DAT3~0(Output of dividing frequency four from ADSC)
112	DAT3	I	Read data from DISC (PAralle output from ADSC)
113	DAT2	I	
114	DAT1	I	
115	DAT0	I	
116	VDD		
117	SCLOCK	I/O	Debugging cereal clock (270 Ω pull up)
118	SDATA	I/O	Debugging cereal data (270 Ω pull up)
119~122	MONI3~0	O	Internal goods title monitor
123	VSS		
124	NEJECT	I	Eject detection
125	5VDD		
126	NTRYCL	I	Tray close detection
127	NDASP	I/O	ATAPI Drive active/ Sulave connection I/O
128	NCS3FX	I	ATAPI host chip selection
129	NCS1FX	I	ATAPI host chip selection
130	VDD		
131	DA2	I/O	ATAPI host address
132	DA0	I/O	ATAPI host address

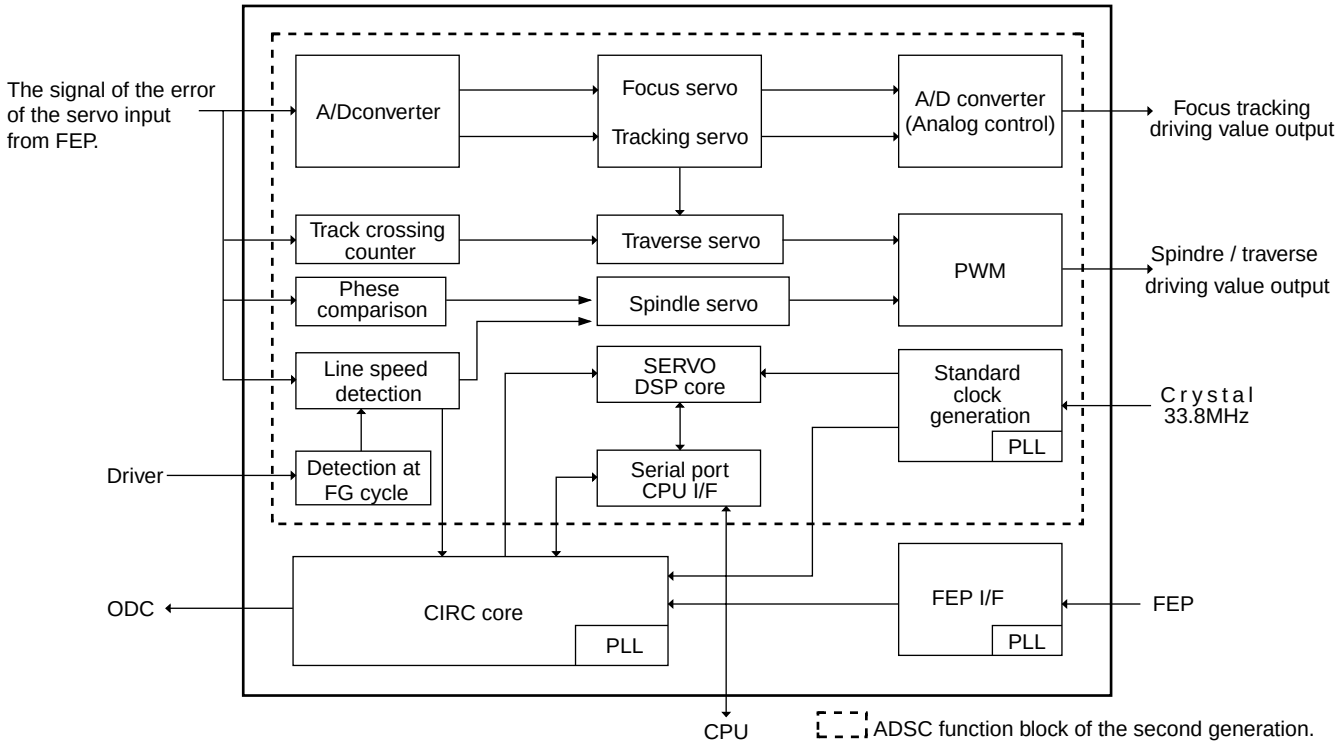
Pin NO.	Symbol	I/O	Function
133	NPDIAG	I/O	ATAPI slave master diagnosis input
134	VSS		
135	DA1	I/O	ATAPI host address
136	IOCS16	O	ATAPI output of selection of width of host data bus
137	INTRQ	O	ATAPI host interruption output
138	5VDD		
139	NDMACK	I	ATAPI host DMA response
140	IORDY	O	ATAPI host ready output
141	NIORD	I	ATAPI host read
142	VSS		
143	NIOWR	I/O	ATAPI host writes
144	DMARQ	O	ATAPI host DMA demand

MN67705EA (IC201) : Digital servo controller

1.Terminal layout



2.Block diagram



3.Pin function

MN67705EA (1/3)

Pin No.	Symbol	I/O	Function
1	FGC	0	H fixation
2	LDONA	O	Laser drive controlA (ON / OFF)
3	LDONB	O	Laser drive controlB (ON / OFF)
4	PULIN	O	DSL and PLL high boost signal (FEP)
5	SRF	O	Head amplifier gain H/L selection
6	DVSS	—	Ground for digital circuit
7	TRAYSET1	O	Tray drive ON/OFF and direction control
8	TRAYSET2	O	Tray drive ON/OFF and direction control
9	DRVMUTE	O	Drive IC mute control
10	DVDD	—	Power supply for digital circuit
11	TRVSW	I	Surroundings position detection in traverse
12	TRAY-CLOSE	I	Tray close detection SW
13	TRAY-OPEN	I	Tray opening detection SW
14	ST/SP	O	Spindle motor drive switch (START /STOP)
15	HFMON	O	High cycle module control
16	BRK	O	Spindle motor IC short brake control
17	DVSS	—	Ground for digital circuit
18	PLLOK	I	SYNC detection (DVD : 18T / CD : 22T)
19	N.C.	O	
20	TBAL(PWMDA1)	O	Tracking balance (FEP)
21	GBAL(PWMDA2)	O	Tangential balance (FEP)
22	BDOLVL(PWMDA3)	O	BDO slice level (FEP)
23	OFTLVL(PWMDA4)	O	Off-track error slice level (FEP)
24	N.C.	O	
25	N.C.	O	
26	N.C.	O	
27	DVSS	—	Ground for digital circuit
28	DVDD	—	Power supply for digital circuit
29	TSTSG	O	Self calibration signal (FEP)
30	FUPDN	O	Signal of frequency UP/DOWN of PLL (FEP)
31	MONA	O	Monitor terminal A
32	MONB	O	Monitor terminal B
33	CPSEN	I	Servo DSP cereal I/F chip selection (SYSCOM)
34	CPCEN	I	CIRC cereal I/F chip selection (SYSCOM)
35	CPUIRQ	O	Interrupt request to silicon (SYSCOM)
36	CPUCLK	I	Silicon cereal I/F clock (SYSCOM)
37	CPUDTIN	I	Silicon cereal I/F data input (SYSCOM)
38	CPUDTOUT	O	Silicon cereal I/F data output (SYSCOM)
39	CHK4I	I	Connects with unused DVSS
40	SCLK+	I	Lead channel clock differential motion signal (positive)
41	SCLK-	I	Lead channel clock differential motion signal (negative)
42	SDAT+	I	Lead channel data differential motion signal (positive)
43	SDAT-	I	Lead channel data differential motion signal (negative)
44	BDO	I	BDO + BCA (FEP)
45	SBCK	I	CD sub-code data shift clock (ODC)
46	IREF2	—	Connects with unused DVSS

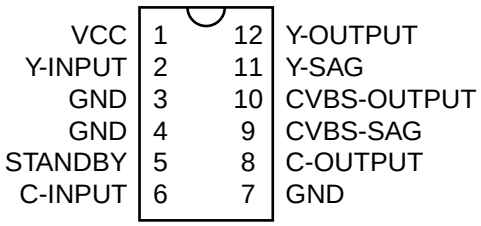
MN67705EA (2/3)

Pin No.	Symbol	I/O	Function
47	IREF3	—	Connects with unused DVSS
48	VCOF2	—	Connects with unused DVSS
49	DVSS	—	Ground for digital circuit
50	VCOE3	—	Connects with unused DVSS
51	DVSS	—	Ground for digital cirucuit
52	DVDD	—	Power supply for digital cirucuit
53	SUBC	O	CD sub-code (ODC)
54	BLKCLK	O	CD sub-code synchronous signal (ODC)/Jump output of one at DVD
55	MONC	O	Monitor terminal C
56	NCLDCK	O	Sub-code data freme clock (ODC)
57	LRCK	O	LR channnel data strove circCIRC(ODC)
58	NTRON	O	L: Tracking ON (ODC)
59	DVSS	—	Ground for digital cirucuit
60	DAT0	O	CIRC / Binary making DVD data output
61	DAT1	O	CIRC / Binary making DVD data output
62	DAT2	O	CIRC / Binary making DVD data output
63	DAT3	O	CIRC / Binary making DVD data output
64	CHCK4	O	Synchronous clock of DAT0～3
65	DVSS	—	Ground for digital circuit
66	DACCLK	O	
67	DACLRCK	I	Connects with unused DVSS
68	DACDATA	I	Connects with unused DVSS
69	CIRCIRQ	O	RAM with built-in CIRC exceeds / Underflow interrupt
70	IPFLAG	O	CIRC error flag
71	MOND	O	Monitor terminal D
72	TX	O	Digital audio interface
73	DVSS	—	Ground for digital cirucuit
74	DVDD	—	Power supply for digital cirucuit
75	AVSS	—	Ground for analog cirucuit
76	VREFLAD	—	AD subordinate position standard voltage (0.6±0.1v)
77	VREFMAD	—	It is a place standard voltage in AD (1.4±0.1V)
78	VREFHAD	—	High-ranking AD standard voltage (2.2±0.1V)
79	AVDD	—	Power supply for analog circuit
80	VREFC(AD12)	I	
81	JIOUT(AD11)	I	Jitter signal(FEP)
82	LDCUR(AD10)	I	Laser drive current signal
83	VREFOP	—	Operation amplifier standard voltage(VREFC)
84	RFENV(AD9)	I	RFENV(FEP)
85	N.C.(AD8)	I	Connects with VREFC
86	N.C.(AD7)	I	Connects with VREFC
87	TG(AD6)	I	Tangential Phase difference (FEP)
88	VREFHDA	—	High-ranking AD standard voltage (2.2±0.1V)
89	VREFMDA	—	It is a place standard voltage in AD (1.4±0.1V)
90	VREFLDA	—	AD subordinate position standard voltage (0.6±0.1v)
91	TE(AD5)	I	Tracking error (FEP)
92	TROFS(AD4)	I	Tracking drive IC input offset
93	FE(AD3)	I	Focus error (FEP)

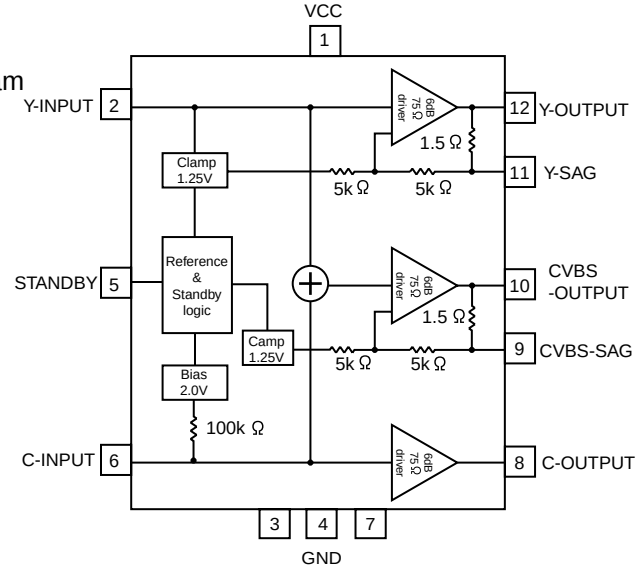
Pin No.	Symbol	I/O	Function
94	FS(AD2)	I	FS (FEP)
95	TS(AD1)	I	TS (FEP)
96	AVSS	—	Ground for analog cirucuit
97	AVDD	—	Power supply for analog circuit
98	FBAL(DA1)	O	Focus balance(FEP)
99	FC(DA2)	O	Cutting off frequency (FEP)
100	BOOST(DA3)	O	Amount of boost (FEP)
101	TBAL(DA4)	O	DSL offset balance (FEP)
102	FODRV(DA5)	O	Focus drive
103	TRDRV(DA6)	O	Tracking drive
104	TRSDRVA(DA7)	O	Traverse drive A aspect
105	TRSDRVB(DA8)	O	Traverse drive B aspect
106	DVDD	—	Power supply for digital cirucuit
107	OFTR	I	Off-track error signal (FEP)
108	TKCRS1	I	Track crossing signal 1 (FEP)
109	TKCRS2	I	Track crossing signal 2 (FEP)
110	DSLO	I	Binary making data slice signal (FEP)
111	FG	I	FG signal input (spindle motor driver)
112	MINTEST	—	Connects with DVSS
113	TEST	—	Connects with DVSS
114	XRESET	I	Reset L : Reset
115	IREF1	—	VCO reference current 1(for SYSCLK)
116	DVSS	—	Ground for digital circuit)
117	VCOF1	—	VCO control voltage 1 (for SYSCLK)
118	SYSCLK	I	33.8MHz system clock input
119	DVSS	—	Ground for digital circuit
120	EC(PWM3A)	O	Spindle motor drive
121	ECR(PWM3B)	O	
122	N.C.(PWM3A)	O	
123	N.C.(PWM2B)	O	
124	N.C.(PWM1A)	O	
125	CDDVD	O	CD/DVD control signal (FEP) CD : H DVD : L
126	N.C.(PWM0A)	O	
127	N.C.(PWM0B)	O	
128	FEPNTRON	O	Tracking ON (FEP)

■ TK15400(IC701):Video AMP.

1.Pin layout

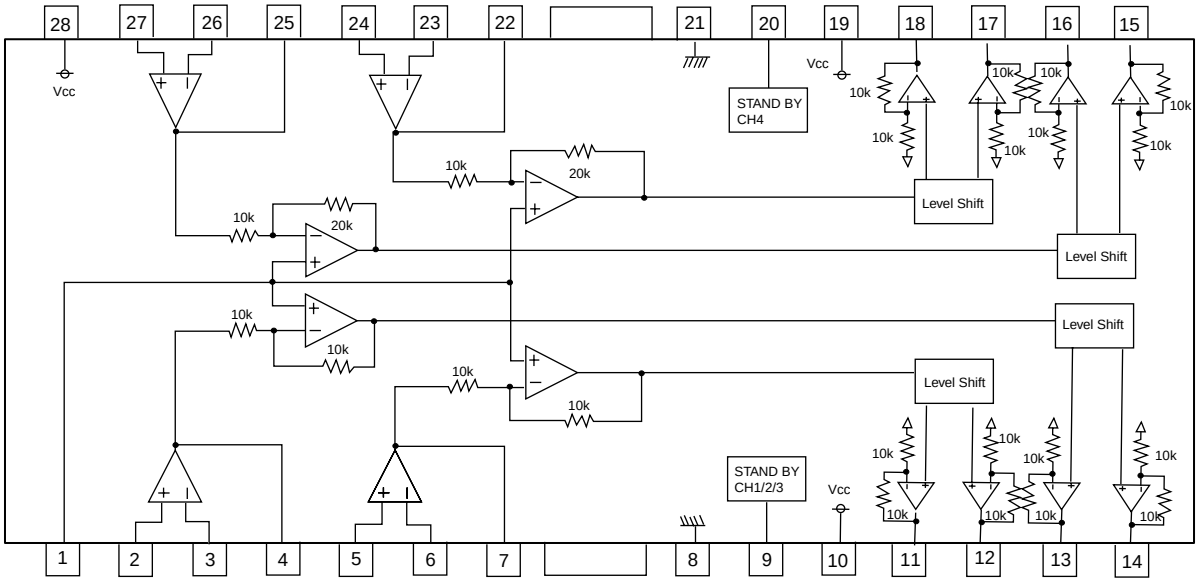


2.Block diagram



■ BA5983FM-X(IC271):4CH driver

1. Block diagram

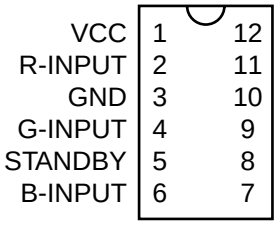


2. Pin function

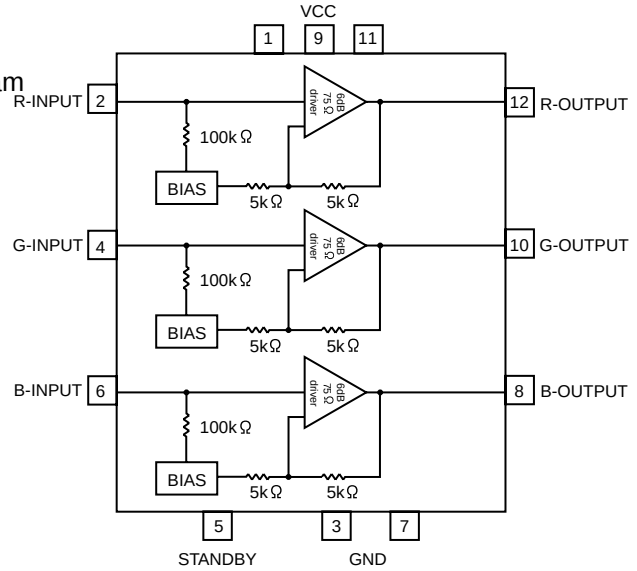
Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	BLAS IN	I	Amplifier input	15	VO4(+)	O	CH4 output (+)
2	OPIN1(+)	I	CH1 amplifier input (+)	16	VO4(-)	O	CH4 output (-)
3	OPIN1(-)	I	CH1 amplifier input (-)	17	VO3(+)	O	CH3 output (+)
4	OPOUT1	O	CH1 amplifier output	18	VO3(-)	O	CH3 output (-)
5	OPIN2(+)	I	CH2 amplifier input (+)	19	PowVcc2	-	CH3/4 power supply
6	OPIN2(-)	I	CH2 amplifier input (-)	20	STBY2	I	CH4 input
7	OPOUT2	O	CH2 amplifier output	21	GND	-	Ground
8	GND	-	Ground	22	OPOUT3	O	CH3 amplifier output
9	STBY1	I	CH1/2/3 input control	23	OPIN3(-)	I	CH3 amplifier input (-)
10	PowVcc1	-	CH1/2 power supply	24	OPIN3(+)	I	CH3 amplifier input (+)
11	VO2(-)	O	CH2 output (-)	25	OPOUT4	O	CH4 amplifier output
12	VO2(+)	O	CH2 output (+)	26	OPIN4(-)	I	CH4 amplifier input (-)
13	VO1(-)	O	CH1 output (-)	27	OPIN4(+)	I	CH4 amplifier input (+)
14	VO1(+)	O	CH1 output (+)	28	PreVcc	-	Power supply pin

■ TK15401(IC702):Video AMP.

1.Pin layout



2.Block diagram



■ MN101C23DBP3 (IC810) : System controller

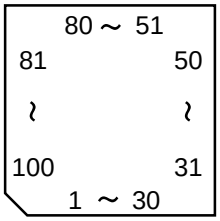
Pin No.	Symbol	I/O	Descriptions
1	KCMND	O	VC3 Serial data output
2	MSTAT	I	VC3 Status data input
3	KCLK	I	VC3 Serial clock input
4	DATAOUT	O	SLC/TUNER data output
5	DATAIN	I	SLC/TUNER data input
6	CK	O	SLC/TUNER clock signal output
7	BEAT	O	BEAT Cut signal output of TUNER
8	VDD	-	Power supply +5V
9,10	OSC2,1	I/O	Oscillation terminal (8MHz)
11	VSS	-	Connect to GND
12,13	XI,XO	I/O	Sub clock (32.768kHz)
14	MMOD	-	Connect to GND
15	VREF-	-	Connect to GND
16~19	KEY1~4	I	Key matrix input 1~4
20	SLCKEY1	I	Tape A playback detect switch
21	SLCKEY2	I	Tape B playback detect switch
22	SLCKEY3	I	Tape B playback/recording detect switch
23	SPIDTI	I	SPI data input
24	VREF+	-	Power supply +5V
25	MRDY	I	VC3 ready input
26	RESET	I	Reset signal input
27	PANEL OP	I	Moving panel open detection signal input
28	PANEL CL	I	Moving panel close detection signal input
29	LOAD DET	I	Overload detect signal input
30	MSI	I	MS Detector signal input
31	PROSACK	O	Clock signal output to IC406
32	PROSADA	I	Data input from IC406
33	REMIN	I	Remote control signal input
34	PHOTOA	I	Tape A mechanism running detection signal input
35	PHOTOB	I	Tape B mechanism running detection signal input
36	INH	I	Inhibit signal input
37	RDSCLK	I	Clock signal input from IC4
38	PRT	I	Protector input
39	RDS DATA	I	RDS data input from IC4
40	SPICSB	O	SPI Chip select signal output
41	OSDCLK	-	Not used
42~44	SPIC~A	O	SPI-C~A Data output to IC542
45,46	VOL+/-	I	Volume rotary encoder input (+/-)
47	MPX	I	Stereo detect
48	FVOLDA	O	Front volume data output
49	SLCCE	O	SLC Chip enable signal output to IC303,IC304
50	RVOLDA	O	Rear volume data output
51~59	G9~1	O	FL grid control signal output
60~89	P1~30	O	FL segment control signal output
90	SABCE	O	SA BASS Chip enable signal output
91	PROCE	O	ProLogic Chip enable signal output
92	DSPCE	O	DSP Chip enable signal output
93	EXTCE	O	EXT Chip enable signal output
94	VOLCK	O	Clock signal output to IC401
95	SMUTE	O	System mute control signal output
96	OSDCE	-	Not used
97	POUT	O	Power ON/OFF
98	TUCE	O	TUNER Chip enable signal output
99	VC3RESET	O	VC3 Reset output
100	VPP	-	Power supply

■ MN102LP25GGB(IC401):UNIT CPU

Pin No.	Symbol	I/O	Function	Pin No.	Symbol	I/O	Function
1	WAIT	I	Micon wait signal input	51	SWCLOSE	I	Detection switch of tray close
2	RE	O	Read enable	52	SWOPEN	I	Detection switch of tray open
3	MUTE	O	Driver mute	53	ADSCEN	O	Serial enable signal for ADSC
4	WEM	O	Write enable	54	VDD	-	Non connect
5	CS0	O	Non connect	55	EFPEN	O	Serial enable signal for FEP
6	CS1	O	Chip select for ODC	56	SLEEP	O	Standby signal for FEP
7	CS2	O	Chip select for ZIVA	57	BUSY	I	Communication busy
8	CS3	O	Chip select for outer ROM	58	REQ	O	Communication Request
9	TCLOSE	O	Tray close signal output	59	WEROM	O	Non connect
10	TOPEN	O	Tray open signal output	60	WPROM	O	Non connect
11	LSIRST	I	LSI reset	61	VSS	-	Power supply
12	WORD	O	Bus selection input	62	EECS	O	Chip select signal for EEPROM
13	A0	O	Address bus 0 for CPU	63	EECK	O	Clock signal for EEPROM
14	A1	O	Address bus 1 for CPU	64	EEDI	I	Input data for EEPROM
15	A2	O	Address bus 2 for CPU	65	EEDO	O	Output data for EEPROM
16	A3	O	Address bus 3 for CPU	66	VDD	-	Power supply
17	VDD	-	Power supply	67	SCLK0	I	Communication clock
18	SYSCLK	O	System clock signal output	68	S2UDT	I	Communication input data
19	VSS	-	Power supply	69	S2SDT	O	Communication output data
20	XI	-	Non connect	70	CPSCK	O	Clock for ADSC serial
21	XO	-	Non connect	71	SDIN	I	ADSC serial data input
22	VDD	-	Power supply	72	SDOUT	O	ADSC serial data output
23	OSCI	I	Clock signal input(13.5MHz)	73	-	-	Non connect
24	OSCO	-	Non connect	74	-	-	Non connect
25	MODE	I	CPU Mode selection input	75	NMI	-	Non connect
26	A4	O	Address bus 4 for CPU	76	ADSCIRQ	I	Interrupt input of ADSC
27	A5	O	Address bus 5 for CPU	77	ODCIRQ	I	Interrupt input of ODC
28	A6	O	Address bus 6 for CPU	78	DECIRQ	I	Interrupt input of ZIVA
29	A7	O	Address bus 7 for CPU	79	WAKEUP	O	Non connect
30	A8	O	Address bus 8 for CPU	80	ODCIRQ2	I	Non connect
31	A9	O	Address bus 9 for CPU	81	ADSEP	I	Address data selection input
32	A10	O	Address bus 10 for CPU	82	RST	I	Reset input
33	A11	O	Address bus 11 for CPU	83	VDD	-	Power supply
34	VDD	-	Power supply	84	TEST1	I	Test signal 1 input
35	A12	O	Address bus 12 for CPU	85	TEST2	I	Test signal 2 input
36	A13	O	Address bus 13 for CPU	86	TEST3	I	Test signal 3 input
37	A14	O	Address bus 14 for CPU	87	TEST4	I	Test signal 4 input
38	A15	O	Address bus 15 for CPU	88	TEST5	I	Test signal 5 input
39	A16	O	Address bus 16 for CPU	89	TEST6	I	Test signal 6 input
40	A17	O	Address bus 17 for CPU	90	TEST7	I	Test signal 7 input
41	A18	O	Address bus 18 for CPU	91	TEST8	I	Test signal 8 input
42	A19	O	Address bus 19 for CPU	92	VSS	-	Power supply
43	VSS	-	Power supply	93	D0	I/O	Data bus 0 of CPU
44	A20	O	Address bus 20 for CPU	94	D1	I/O	Data bus 1 of CPU
45	-	-	Non connect	95	D2	I/O	Data bus 2 of CPU
46	STOP	-	Non connect	96	D3	I/O	Data bus 3 of CPU
47	ADPD	-	Non connect	97	D4	I/O	Data bus 4 of CPU
48	-	-	Non connect	98	D5	I/O	Data bus 5 of CPU
49	-	-	Non connect	99	D6	I/O	Data bus 6 of CPU
50	TRVSW	I	Detection switch of traverse inside	100	D7	I/O	Data bus 7 of CPU

■ JCV8005-2(IC351):CPPM

1.Pin layout



2.Pin function

JCV8005-2 1/2

Pin No.	Symbol	I/O	Description
1	VDD	-	Power supply
2	GND	-	Connect to ground
3~10	HDATA0~7	I/O	Data input/output terminal (both by 8 bits)
11	VDD	-	Power supply
12	GND	-	Connect to ground
13~20	HADDR0~7	I	8 bit address bus to internal address (connect to host)
21	VDD	-	Power supply
22	GND	-	Connect to ground
23	NCS	I	Chip select signal from host
24	NRD	I	Data read signal from host
25	NWR	I	Data write signal from host
26	NIRQ	O	Interrupt of request to host
27	WAIT	O	Wait demand to host
28	NRESET	I	Reset signal from host
29	VDD	-	Power supply
30	GND	-	Connect to ground
31	VDD	-	Power supply
32	GND	-	Connect to ground
33~36	STD7~4_OUT	O	Data output to DVD decoder (8 bits)
37	GND	-	Connect to ground
38~41	STD3~0_OUT	O	Data output to DVD decoder (8 bits)
42	VDD	-	Power supply
43	GND	-	Connect to ground
44	REQ_IN	I	Request signal for forwarding control by decoder
45	DACK_OUT	O	Output signal to decoder which shows effective data
46	STCLK_OUT	O	Data strobe signal to decoder
47	SYNC_OUT	O	Sector sink signal to decoder
48	STERROUT	-	Non connect
49	VDD	-	Power supply
50	GND	-	Connect to ground
51	VDD	-	Power supply
52	GND	-	Connect to ground
53	NG_RD	I	Glue logic input signal from host
54	NG_WR	I	Glue logic input signal from host
55	G_WITODC	I	Glue logic input signal from front end
56	G_CSDEC	I	Glue logic input signal from host
57	G_WITDEC	I	Glue logic input signal from decoder
58	VDD	-	Power supply
59	GND	-	Connect to ground
60	WAIT1	O	Glue logic output signal to host

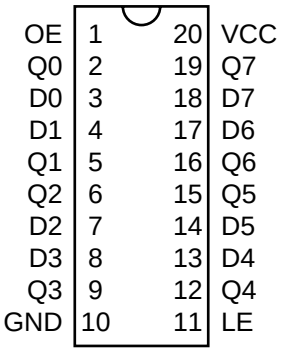
2.Pin function

JCV8005-2 2/2

Pin No.	Symbol	I/O	Description
61	WAIT2	-	Non connect
62	WAITIN	I	Glue logic input signal (connect to 27 pin)
63	VDD	-	Power supply
64	GND	-	Connect to ground
65	TEST_IN	I	Connect to ground
66,67	NC	-	Non connect
68	VDD	-	Power supply
69	GND	-	Connect to ground
70	CLKOCTL	I	Input terminal for crystal-oscillator circuit on/off control
71	NC	-	Non connect
72	OSCI	I	Crystal oscillation terminal (input side)
73	OSCO	O	Crystal oscillation terminal (output side)
74	NC	-	Non connect
75	VDD	-	Power supply
76	GND	-	Connect to ground
77	33OUT	O	Oscillation output terminal
78	16OUT	O	Oscillation output terminal
79	VDD	-	Power supply
80	GND	-	Connect to ground
81	VDD	-	Power supply
82	GND	-	Connect to ground
83	STERR_IN	I	Presence of data error from front end
84	SYNC_IN	I	Sector sink signal from front end
85	STCLK_IN	I	Data clock signal from front end
86	DACK_IN	I	Signal which shows effective data from front end
87	REQ_OUT	O	Request signal for forwarding control to front end
88	VDD	-	Power supply
89	GND	-	Connect to ground
90~93	STD0~3_IN	I	Data input from front end (8 bits)
94	GND	-	Connect to ground
95~98	STD4~7_IN	I	Data input from front end (8 bits)
99	VDD	-	Power supply
100	GND	-	Connect to ground

■ TC74LCX373FT-X(IC512,IC513)

1.Pin layout



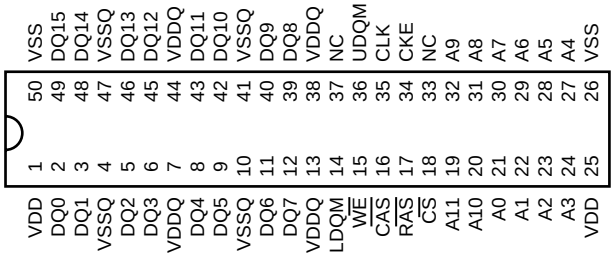
2.Truth table

INPUTS			OUTPUTS
OE	LE	D	
H	X	X	Z
L	L	X	Qn
L	H	L	L
L	H	H	H

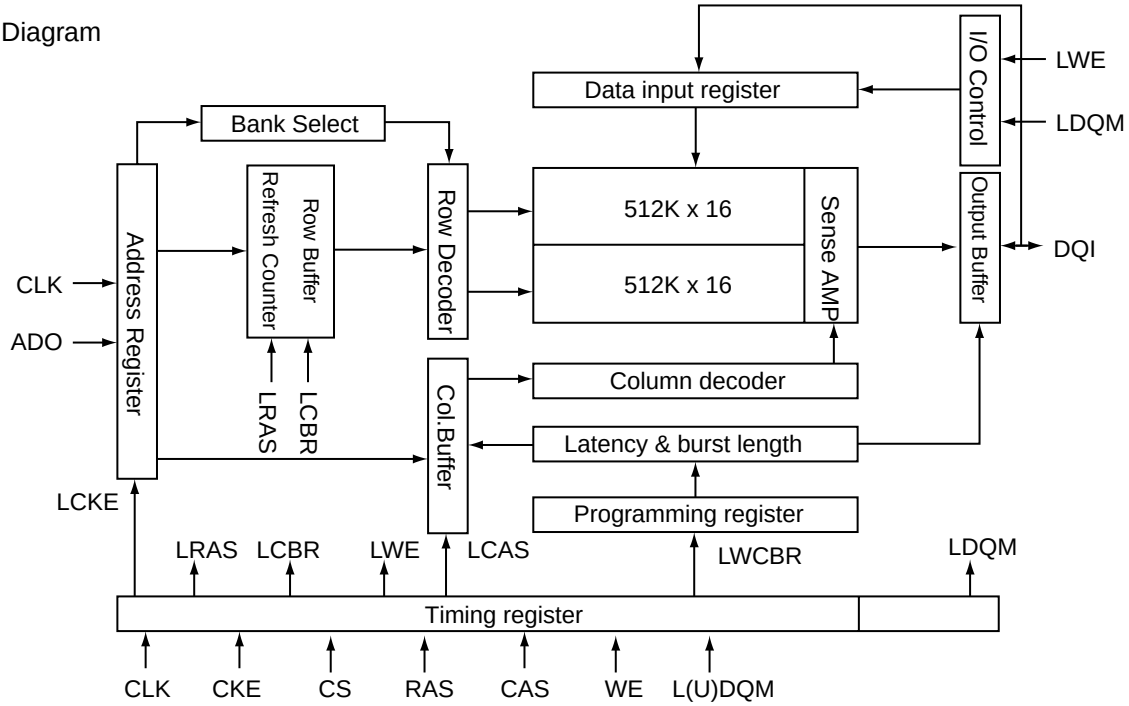
X : Don't care
Z : High impedance
Qn : Q outputs are latched at the time when the LE input is taken to a low logic level.

■ KM416S1120DT-G8(IC504,IC505,IC506,IC507):DRAM

1.Terminal Layout



2.Block Diagram

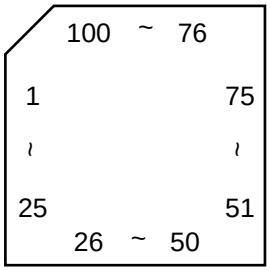


3.Pin Function

Pin No.	Symbol	Function	Pin No.	Symbol	Function
1	VDD	Power Supply	26	VSS	To Ground
2	DQ0	Data Input/Output	27	A4	Address
3	DQ1	Data Input/Output	28	A5	Address
4	VSSQ	To Ground	29	A6	Address
5	DQ2	Data Input/Output	30	A7	Address
6	DQ3	Data Input/Output	31	A8	Address
7	VDDQ	Power Supply	32	A9	Address
8	DQ4	Data Input/Output	33	NC	Non Connection
9	DQ5	Data Input/Output	34	CKE	Clock Enable
10	VSSQ	To Ground	35	CLK	System Clock
11	DQ6	Data Input/Output	36	UDOM	Data Input/Mask Output
12	DQ7	Data Input/Output	37	NC	Non Connection
13	VDDQ	Power Supply	38	VDDQ	Power Supply
14	LDQM	Data Input/Mask Output	39	DQ8	Data Input/Output
15	$\overline{WE}$	Write Enable	40	DQ9	Data Input/Output
16	$\overline{CAS}$	Column Address Strobe	41	VSSQ	To Ground
17	$\overline{RAS}$	Raw Address Strobe	42	DQ10	Data Input/Output
18	$\overline{CS}$	Chip Select	43	DQ11	Data Input/Output
19	A11	Address	44	VDDQ	Power Supply
20	A10	Address	45	DQ12	Data Input/Output
21	A0	Address	46	DQ13	Data Input/Output
22	A1	Address	47	VSSQ	To Ground
23	A2	Address	48	DQ14	Data Input/Output
24	A3	Address	49	DQ15	Data Input/Output
25	VDD	Power Supply	50	VSS	To Ground

■MN101C35DGA(IC901):Front Controller

1.Terminal Layout

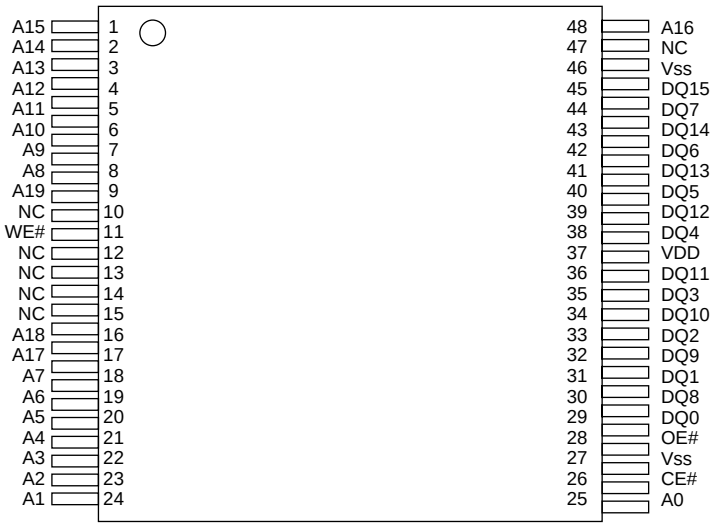


2.Pin Function

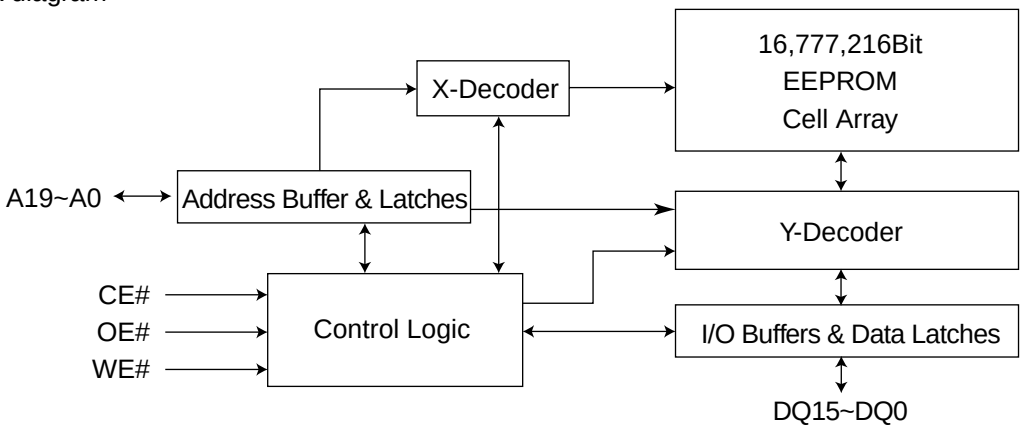
Pin No.	Symbol	I/O	Function
1	TXD	O	Serial Data Output
2	RXD	I	Serial Data Input
3	SCK	I	Serial Clock
4,5	P04,P05	-	Non Connection
6	POWERON	O	FL Display Power Control
7	RESET	I	Reset Signal Input
8	VDD	-	Power Supply
9,10	OSC1,2	I	Oscillator Terminal
11	VSS	-	To Ground
12	X1	-	To Ground
13	X0	-	Non Connection
14	MMOD	-	To Ground
15	VREF-	-	To Ground
16~23	AN0~7	-	To Ground
24	VREF+	-	Power Supply
25	P07	-	Non Connection
26	RST	I	Reset Signal
27~29	KEYI0~2	I	Key Matrix Input 0~2
30,31		-	To Ground
32	MUTE	O	Muting control Output
33	REMO		
34	AVCI		
35	CS	I	Chip Select Input
36~38	P23~P25	-	Non Connection
39~41		-	To Ground
42~44	KEYO0~2	O	Key Matrix Output 0~2
45	KEYO3	-	Non Connection
46	P54	-	Non Connection
47	DOFFIND	O	DISPLAY OFF Indicator Control
48	STANDBYIND	O	STANDBY Indicator Control
49	AUDIOIND	O	DVD AUDIO Indicator Control
50	44IND	O	DIGITAL DIRECT PROGRESSIVE Indicator Control
51	48IND	O	44.1kHz/48kHz Indicator Control
52	96IND	O	88.2kHz/96kHz Indicator Control
53	192IND	O	176.4kHz/192kHz Indicator Control
54~64	DGT10~0	O	FL Grid Control Signal Output
65~72	SEG27~34	O	FL Segment Control Signal Output
73~99	SEG0~26	O	FL Segment Control Signal Output
100	VPP	-	Power Supply

■ SST39VF160 (IC508,509) : 16M EEPROM

1. Pin layout



2. Block diagram



3. Pin function

Symbol	Pin name	Function
A19~A0	Address Inputs	To provide memory addresses. During sector erase A19~A11 address lines will select the sector. During block erase A19~A15 address lines will select the block.
DQ15~DQ0	Data Input/Output	To output data during read cycles and receive input data during write cycles. Data is internally latched during a write cycle. The outputs are in tri-state when OE# or CE# is high.
CE#	Chip Enable	To activate the device when CE# is low.
OE#	Output Enable	To gate the data output buffers.
WE#	Write Enable	To control the write operations.
VDD	Power Supply	To provide 3-volt supply (2.7V-3.6V).
Vss	Ground	
NC	No Connection	Unconnected pins.

<<MEMO>>

XV-D721BK
XV-D723GD

JVC

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